Quad 2-Input NAND Gate with Schmitt-Trigger Inputs with LSTTL Compatible Inputs

High–Performance Silicon–Gate CMOS

The MC74HCT132A is identical in pinout to the LS132. The device inputs are compatible with standard CMOS outputs; with pull–up resistors, they are compatible with LSTTL outputs.

The MC74HCT132A can be used to enhance noise immunity or to square up slowly changing waveforms.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 µA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements as Defined by JEDEC Standard No. 7A
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

A1 [1●	14	l v _{cc}
B1 [2	13] в4
Y1 [3	12	D A4
A2 [4	11	D Y4
В2 [5	10	🛛 вз
Y2 [6	9	а П
GND [7	8	IY3





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MARKING DIAGRAMS



14 <u>A A A</u>	AAAA	
HCT 132A		

A = Assembly Location WL, L = Wafer Lot Y = Year WW, W = Work Week

G or • = Pb–Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Inp	Inputs		
Α	В	Y	
L	L	Н	
L	н	н	
н	L	н	
н	Н	L	

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

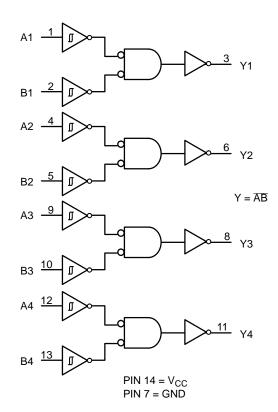


Figure 2. Logic Diagram

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74HCT132ADG		55 Units / Rail
MC74HCT132ADR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
NLV74HCT132ADR2G*		2500 / Tape & Reel
MC74HCT132ADTR2G	TSSOP-14	2500 / Tape & Reel
NLVHCT132ADTR2G*	(Pb-Free)	2500 / Tape & Reel

For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP

Capable.

MAXIMUM RATINGS

Symbol	Pa	Value	Unit	
V _{CC}	Positive DC Supply Voltage		-0.5 to +7.0	V
V _{IN}	Digital Input Voltage		-0.5 to +7.0	V
V _{OUT}	DC Output Voltage	Output in 3–State High or Low State	-0.5 to +7.0 $-0.5 \text{ to V}_{CC} +0.5$	V
I _{IK}	Input Diode Current		-20	mA
I _{OK}	Output Diode Current		±20	mA
I _{OUT}	DC Output Current, per Pin		±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pir	าร	±75	mA
I _{GND}	DC Ground Current per Ground Pin		±75	mA
T _{STG}	Storage Temperature Range		-65 to +150	°C
ΤL	Lead Temperature, 1 mm from Case for	or 10 Seconds	260	°C
ТJ	Junction Temperature Under Bias		+ 150	°C
θ_{JA}	Thermal Resistance	14–SOIC 14–TSSOP	125 170	°C/W
P _D	Power Dissipation in Still Air at 85°C	SOIC TSSOP	500 450	mW
MSL	Moisture Sensitivity		Level 1	
F _R	Flammability Rating	Oxygen Index: 30% – 35%	UL 94 V0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	>2000 >100 >500	V
I _{Latch-Up}	Latch–Up Performance	Above V _{CC} and Below GND at 85 $^{\circ}$ C (Note 4)	±300	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. 1. Tested to EIA/JESD22–A114–A.

2. Tested to EIA/JESD22-A115-A.

3. Tested to JESD22-C101-A.

4. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	- 55	+ 125	°C
t _r , t _f	Input Rise and Fall Time (Figure 3)	-	No Limit (Note 5)	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

When V_{IN} ~ 0.5 V_{CC}, I_{CC} >> quiescent current.
Unused inputs may not be left open. All inputs must be tied to a high–logic voltage level or a low–logic input voltage level.

			V _{CC}	Guaranteed Limit			
Symbol	Parameter	Test Conditions	v	−55°C to 25°C	≤85°C	≤125°C	Unit
V _{T+} max	Maximum Positive–Going Input Threshold Voltage	$ \begin{array}{l} V_{OUT} = 0.1 \ V \\ I_{OUT} \ \leq \ 20 \ \mu A \end{array} $	4.5 5.5	1.9 2.1	1.9 2.1	1.9 2.1	V
V _{T+} min	Minimum Positive–Going Input Threshold Voltage	$ \begin{array}{l} V_{OUT} = 0.1 \ V \\ I_{OUT} \ \leq \ 20 \ \mu A \end{array} $	4.5 5.5	1.2 1.4	1.2 1.4	1.2 1.4	V
V _T _max	Maximum Negative–Going Input Threshold Voltage	$\begin{array}{l} V_{OUT} = V_{CC} - 0.1 \ V \\ I_{OUT} \leq 20 \ \mu A \end{array} \end{array} \label{eq:Vout}$	4.5 5.5	1.2 1.4	1.2 1.4	1.2 1.4	V
V_{T-} min	Minimum Negative–Going Input Threshold Voltage	$\label{eq:VOUT} \begin{array}{l} V_{OUT} = V_{CC} - 0.1 \ V \\ I_{OUT} \leq 20 \ \mu A \end{array}$	4.5 5.5	0.5 0.6	0.5 0.6	0.5 0.6	V
V _H min (Note 7)	Minimum Hysteresis Voltage	$\begin{array}{l} V_{OUT} = 0.1 \ V \ or \ V_{CC} - 0.1 \ V \\ I_{OUT} \ \leq \ 20 \ \mu A \end{array}$	4.5 5.5	0.4 0.4	0.4 0.4	0.4 0.4	V
V _{OH}	Minimum High–Level Output Voltage	$\begin{array}{ll} V_{IN} \leq & V_{T_} \text{min or } V_{T_} \text{max} \\ I_{OUT} \leq 20 \ \mu \text{A} \end{array}$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		$V_{IN} \leq -V_{T_{-}}$ min or $V_{T_{+}}$ max $ I_{OUT} \leq 4.0 \text{ mA}$	4.5	3.98	3.84	3.7	
V _{OL}	Maximum Low–Level Output Voltage	$V_{IN} \ge V_{T+}max$ $ I_{OUT} \le 20 \mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		$V_{IN} \ge V_{T+}max$ $ I_{OUT} \le 4.0 mA$	4.5	0.26	0.33	0.4	
I _{IN}	Maximum Input Leakage Current	$V_{IN} = V_{CC}$ or GND	5.5	±0.1	±1.0	±1.0	μΑ
I _{CC}	Maximum Quiescent Supply Current (per Package)	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \ \mu A$	5.5	1.0	10	40	μA

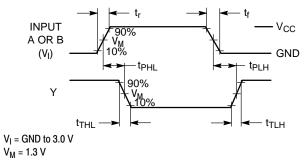
DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 7. $V_Hmin > (V_{T_+}min) - (V_{T_-}max); V_Hmax = (V_{T_+}max) + (V_{T_-}min).$

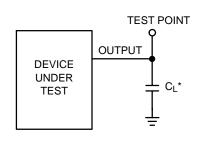
AC ELECTRICAL CHARACTERISTICS (CL = 50 pF, Input tr = tf = 6.0 ns, V_{CC} = 5.0 V \pm 10%)

		V _{CC}	Guaranteed Limit			
Symbol	Parameter	v	−55°C to 25°C	≤ 85 °C	≤125°C	Unit
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 3 and 4)	5.0	25	31	38	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 4)	5.0	15	19	22	ns
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
			Typical @ 25°C, V _{CC} = 5.0 V			
C _{PD}	Power Dissipation Capacitance (per Gate) (Note 8)			24		pF

8. Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.







*Includes all probe and jig capacitance



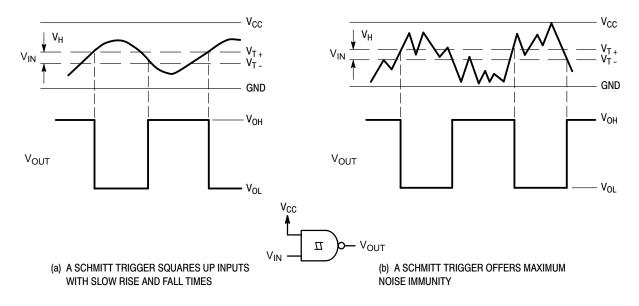
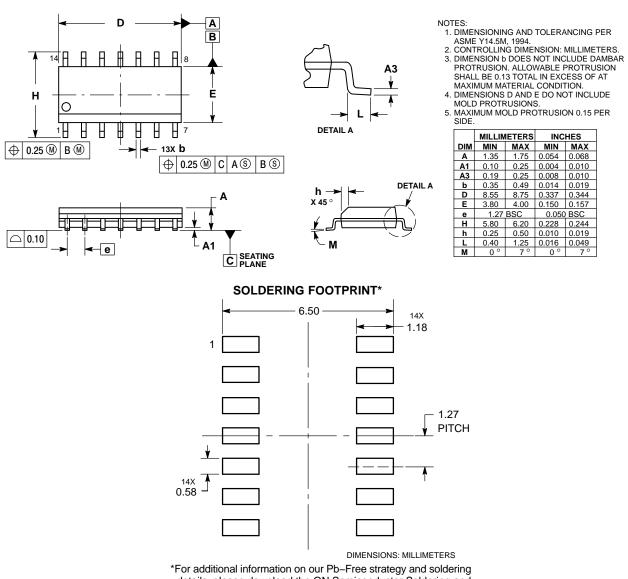


Figure 5. Typical Schmitt-Trigger Applications

PACKAGE DIMENSIONS

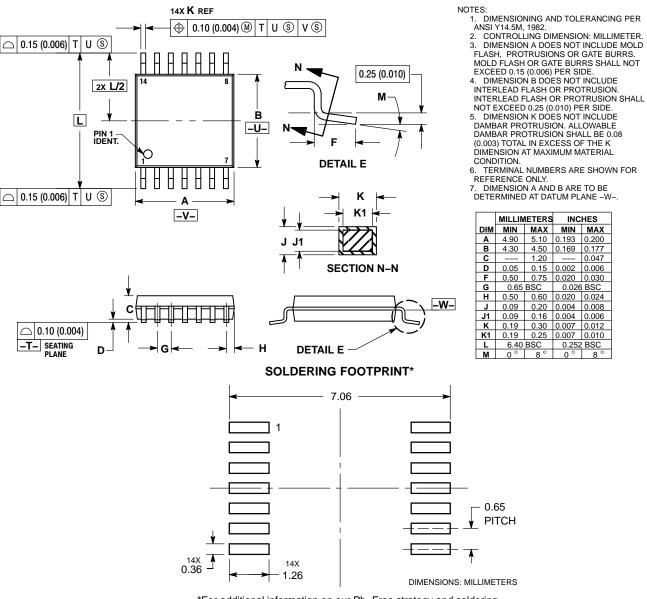
SOIC-14 NB CASE 751A-03 ISSUE L



details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TSSOP-14 WB CASE 948G **ISSUE C**



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MILLIMETERS

0.65 BSC

6.40 BSC

<u>8</u>°

4.90

INCHES

0.026 BSC

0.252 BSC

0

5.10 0.193 0.200

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