MT2502A SOC Processor Technical Brief

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Specifications are subject to change without notice.

Table of Contents

Lists of Tables and Figures

1 System Overview

MT2502A is a monolithic chip integrating leading edge power management unit, analog baseband and radio circuitry based on the low-power CMOS process.

MT2502A is a feature-rich and extremely powerful single-chip solution for high-end GSM/GPRS (2G) capability. Based on the 32-bit ARM7EJ-S™ RISC processor, MT2502A's superb processing power, along with high bandwidth architecture and dedicated hardware support, provides a platform for high-performance GPRS Class 12 MODEM application and leading-edge multimedia applications.

MT2502A also features:

- A highly integrated Bluetooth transceiver which is fully compliant with Bluetooth specification v4.0.
- A FM receiver supporting both audio broadcast de-modulation and RDS/RBDS data decoding.

Typical application diagram is shown in Figure 1.

Platform

MT2502A is capable of running the ARM7EJ-S™ RISC processor, which provides the best trade-off between system performance and power consumption.

For large amounts of data transfer, high-performance DMA (Direct Memory Access) with hardware flow control is implemented, which greatly enhances the data movement speed while reducing the MCU processing load.

Targeted as a media-rich platform for mobile applications, MT2502A also provides hardware security digital rights management for copyright protection. For further safeguard and to protect the manufacturer's development investment, hardware flash content protection is provided to prevent unauthorized porting of the software load.

Memory

MT2502A supports serial flash interface with various operating frequencies.

Multimedia

The MT2502A multimedia subsystem provides serial interface for CMOS sensors. The camera resolution is up to VGA size. The software-based codec can be used to process various video types. To take advantage of the high MCU performance, GIF and PNG decoders are implemented by the software.

In addition, MT2502A is implemented with a high-performance audio synthesis technology, as well as a high-quality audio amplifier to provide superior audio experiences.

Connectivity and storage

MT2502A supports UART, USB 1.1 FS/LS , SDIO and SD storage systems. These interfaces provide MT2502A users with the highest level of flexibility in implementing high-end solutions.

To achieve a complete user interface, MT2502A also brings together all the necessary peripheral blocks for a multimedia wearable product. The peripheral blocks include the keypad scanner with the capability to detect multiple key presses,

SIM controller, real-time clock, PWM, serial LCD controller and general-purpose programmable I/Os.

Audio

Using a highly integrated mixed-signal audio front-end, the MT2502A architecture provides easy audio interfacing with direct connection to the audio transducers. The audio interface integrates A/D converters for voice band, as well as high-resolution stereo D/A converters for both audio and voice band.

MT2502A supports AMR codec to adaptively optimize the quality of speech and audio. Moreover, HE-AAC codec is implemented to deliver CD-quality audio at low bit rates.

In addition, an audio amplifier is also embedded to save the BOM cost of adopting external amplifiers.

GSM/GPRS (2G) radio

MT2502A integrates a mixed-signal baseband front-end in order to provide a well-organized radio interface with flexibility for efficient customization. The front-end contains gain and offset calibration mechanisms and filters with programmable coefficients for comprehensive compatibility control on RF modules. MT2502A achieves outstanding MODEM performance by utilizing a highly dynamic range ADC in the RF downlink path.

MT2502A embeds a high-performance and completely integrated single-ended SAW-less RF transceiver for multi-band GSM cellular system. In this RF transceiver, a quad-band receiving feature with high sensitivity is supported utilizing one RF receiver and a fully integrated channel filter. With ultra-high dynamic range, the off-chip balun and SAW filters on the receiving path can be removed for BOM cost reduction. In addition, the minimum component count is guaranteed by realizing a highly integrated transmitter, low-spur frequency synthesizer and a Digitally-Controlled Crystal Oscillator (DCXO).

Bluetooth radio

MT2502A offers a highly integrated Bluetooth radio and baseband processor. Only a minimum of external components are required. MT2502A provides superior sensitivity and class 1 output power and thus ensures the quality of the connection with a wide range of Bluetooth devices.

MT2502A is fully compliant with Bluetooth v4.0, including BR/EDR and BT low energy and offers enhanced data rates of up to 3Mbps. It also provides the coexistence protocol with 802.11 system.

MT2502A supports rich Bluetooth profiles, enabling diversified applications that are widely used on the handset with excellent interoperability.

FM radio

The FM radio subsystem provides a completely integrated FM Rx receiver supporting 65 ~ 108MHz FM bands with 50kHz tuning step. In addition to receiving FM audio broadcasting, the digital RDS/RBDS data system is supported as well. The integrated FM transceiver utilizes state-of-the-art digital demodulation/modulation techniques to achieve excellent performance.

In order to achieve high SINAD, good sensitivity and excellent noise suppression, the FM receiver adopts adaptive demodulation scheme to optimize Rx system performance in all ranges of

signal quality by reference of a very sophisticated channel quality index (CQI). When the received signal quality is poor, the design not only enhances the ACI rejection capability but also uses a very ingenious skill to soft mute annoying noise so as to provide good perception quality.

The FM radio subsystem supports both long antenna, which is usually an earphone, and auto-calibrated short antenna, which is usually a FPC short antenna or shared antenna with GSM for different application scenarios.

Debugging function

The JTAG interface enables in-circuit debugging of the software program with the ARM7EJ-S™ core. With this standardized debugging interface, MT2502A provides developers with a wide set of options in choosing ARM development kits from different third party vendors.

Power management

A power management is embedded in MT2502 to provide rich features a high-end wearable product supports, including Li-ion battery charger, high performance and low quiescent current LDOs, and drivers for LED and backlight.

MT2502A offers various low-power features to help reduce the system power consumption. MT2502A is also fabricated in an advanced low-power CMOS process, hence providing an overall ultra-low leakage solution.

Package

The MT2502A device is offered in a 5.4mm×6.2mm, 143-ball, 0.4mm pitch, TFBGA package.

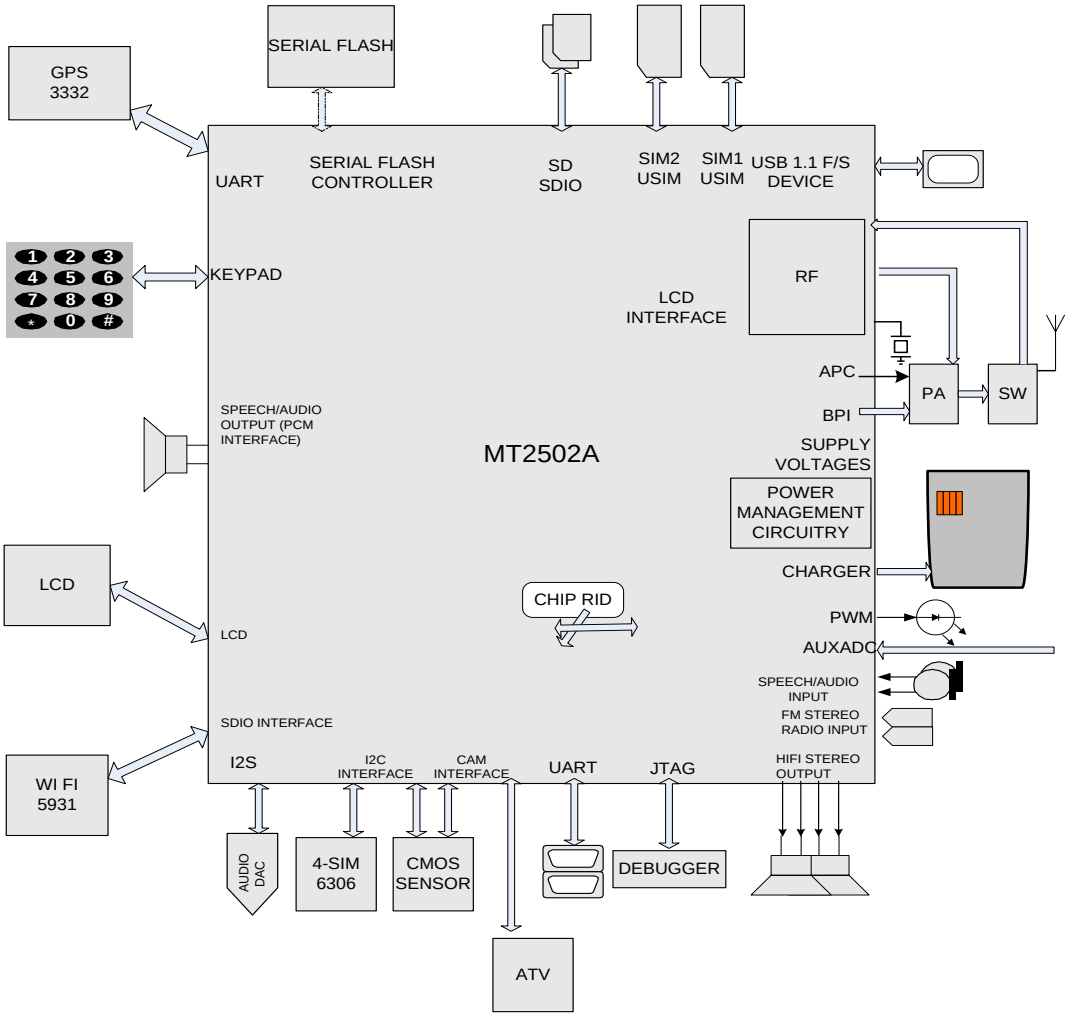


Figure 1. Typical application of MT2502A

1.1 Platform Features

General

- Integrated voice-band, audio-band and base-band analog front-end
- Integrated full-featured power management unit

MCU subsystem

- ARM7EJ-S™ 32-bit RISC processor
- Java hardware acceleration for fast Java-based games and applets
- High-performance multi-layer AHB bus
- Dedicated DMA bus with 16 DMA channels
- On-chip boot ROM for factory flash programming
- Watchdog timer for system crash recovery
- 3 sets of general-purpose timers
- Circuit switch data coprocessor
- Division coprocessor

Serial flash interfaces

- Supports various operating frequency combinations for serial flash
- Supports QPI and SPI serial flash

User interfaces

- 5-row x 5-column keypad controller with hardware scanner
- Supports multiple key presses for gaming
- Dual SIM/USIM controller with hardware T = 0/T = 1 protocol control
- Real-time clock (RTC) operating with a low-quiescent-current power supply
- General-purpose I/Os (GPIOs) available for auxiliary applications
- 2 sets of Pulse Width Modulation (PWM) output
- 24 external interrupt lines
- 1 external channel auxiliary 10-bit A/D converter

Security

- Supports security key and chip random ID

Connectivity

- 3 UARTs with hardware flow control and supports baud rate up to 921,600 bps
- FS/LS USB 1.1 device controller
- Multimedia card, secure digital Memory Card, host controller with flexible I/O voltage power
- Supports 4-bit SDIO interface for SDIO peripherals as well as WIFI connectivity
- DAI/PCM and I2S interface for audio applications
- I2C master interface for peripheral management including image sensors
- SPI master/slave interface for peripheral management.

Power management

- Li-ion battery charger
- 13 LDOs for the power supply of memory card, camera, Bluetooth, RF, SIM card and other diversified usage
- 1 open-drain output switches to supply/control the LED
- LDO type vibrator
- One NMOS switch to control keypad LED
- Thermal overload protection
- Under-voltage lock-out protection

- Over-voltage protection
- Different levels of power-down modes with sophisticated software control enables excellent power saving performance.

Test and debugging

- Built-in digital and analog loop back modes for both audio and baseband front-end
- DAI port complies with GSM Rec.11.10.
- JTAG port for debugging embedded MCU

1.2 Always-on Mode

MT2502A provides always-on mode to optimize the low power performance for wearable device.

A tiny system is built in, it can provide basic always-on function such as clock update, pedometer etc.

MT2502A provides two operation modes, AP mode and always-on mode.

- AP mode
  - Legacy apps
- Always-on mode
  - Basic connecting function
  - Basic sensing function
  - Basic watch function

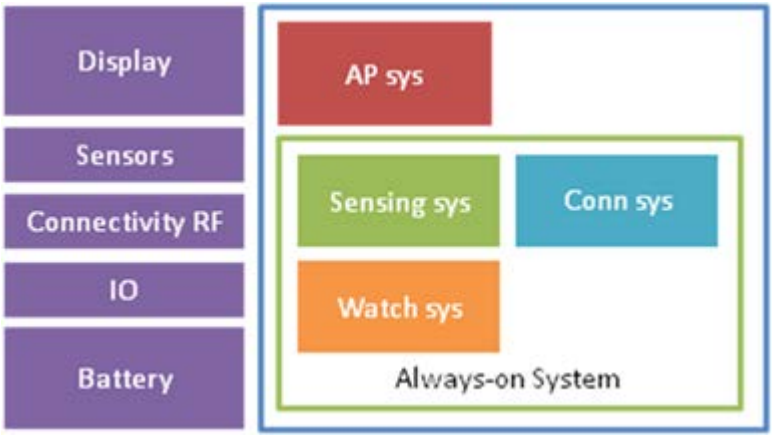


Figure 2. A tiny system on MT2502A

1.3 MODEM Features

Radio interface and baseband front-end

- Digital PM data path with baseband front-end
- High dynamic range delta-sigma ADC converts the downlink analog I and Q signals to digital baseband.
- 10-bit D/A converter for Automatic Power Control (APC)
- Programmable radio Rx filter with adaptive gain control
- Dedicated Rx filter for FB acquisition
- 6-pin Baseband Parallel Interface (BPI) with programmable driving strength
- Supports multi-band

Voice and modem CODEC

- Dial tone generation
- Voice memo
- Noise reduction
- Echo suppression
- Advanced sidetone oscillation reduction
- Digital sidetone generator with programmable gain
- Two programmable acoustic compensation filters
- Supports GSM/GPRS (2G) modem
- GSM quad vocoders for adaptive multirate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
- GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering
- GPRS GEA1, GEA2 and GEA3 ciphering
- GPRS packet switched data with CS1/CS2/CS3/CS4 coding schemes
- GPRS Class 12
- Supports SAIC (single antenna interference cancellation) technology
- Supports VAMOS(Voice services over Adaptive Multi-user channels on One Slot) technology in R9 spec.

Voice interface and voice front-end

- Microphone input has one low-noise amplifier with programmable gain and Automatic Gain Control (AGC) mechanisms
- Voice power amplifier with programmable gain
- 2nd order Sigma-Delta A/D converter for voice uplink path
- Shares D/A converter with audio playback path
- Supports full-duplex hands-free operation
- Compliant with GSM 03.50

1.4 GSM/GPRS RF Features

Receiver

- Dual single-ended LNAs support Quad bandQuadrature RF mixer
- Fully integrated channel filter
- High dynamic range ADC
- 12dB PGA gain with 6dB gain step

Transmitter

- Transmitter outputs support quad bands.
- Highly precise and low noise RF transmitter for GSM/GPRS (2G) applications

Frequency synthesizer

- Programmable fractional-N synthesizer
- Integrated wide range RFVCO
- Integrated loop filter
- Fast settling time suitable for multi-slot GPRS (2G) applications

Digitally-Controlled Crystal Oscillator (DCXO)

- Two-pin 26MHz crystal oscillator
- On-chip programmable capacitor array for coarse-tuning
- On-chip programmable capacitor array for fine-tuning
- Low power mode supports 32K crystal removal

1.5 Multimedia Features

LCD controller

- Supports simultaneous connection to serial 2 lane LCD modules
- LCM formats supported: RGB565, RGB666, RGB888
- Supports LCD module with maximum resolution up to 320x240
- Per pixel alpha channel
- True color engine
- Supports hardware display rotation
- Capable of combining display memories with up to 4 blending layers

Camera interface

- YUV422 format image input
- Capable of processing image of size up to VGA (Mediatek serial interface)

JPEG decoder

- Baseline JPEG decoding
- Supports various YUV formats, DC/AC Huffman tables and quantization tables

JPEG encoder

- ISO/IEC 10918-1 JPEG baseline mode
- ISO/IEC 10918-2 compliance
- Supports YUV420 and grayscale formats
- Supports EXIF/JFIF
- Standard DC and AC Huffman tables
- Provides 5 levels of encode quality
- Supports zeros shutter delay

MJPEG

- Decode spec: CIF@30fps
- Encode spec: QVGA@15fps

Image data processing

- Supports 4x digital zoom
- High throughput hardware scaler. Capable of tailoring an image to an arbitrary size.
- Horizontal scaling with bilinear interpolation
- Vertical scaling with bilinear interpolation
- YUV and RGB color space conversion
- RGB/YCbCr format thumbnail output

MPEG-4/H.263 CODEC

- Software-based MPEG4 encoder
- Software-based MPEG4 decoder
- ISO/IEC 14496-2 simple profile:
  - Decode spec: 480x320@25fps
  - Encode spec: QVGA@15fps
- ISO/IEC 14496-2 advanced simple profile:
  - Decode @ level 0/1/2/3
  - ITU-T H.263 profile 0 @ level 40
- Supports visual tools for decoder: I-VOP, P-VOP, B-VOP, AC/DC prediction, 4-MV, unrestricted MV, error resilience, short header, global motion compensation, method 1/2 quantization, quarter-pel motion compensation.
- Error resilience for decoder: Slice resynchronization, data partitioning, reversible VLC
- Supports visual tools for encoder: I-VOP, P-VOP, Half-Pel, DC prediction, unrestricted MV, short header

H.264

- ISO/IEC 14496-10 baseline profile
  - Decode spec: QCIF@30fps

2D accelerator

- Supports 32-bpp ARGB8888, 24-bpp RGB888, 16-bpp RGB565, 24-bpp ARGB6666.
- 4 layers overlay with individual color format, window size, source key, constant alpha and rotation
- Rectangle fill with constant
- BitBlt: Capable with 7 rotation types
- Alpha blending with 7 rotation types, per-pixel alpha and pre-multiplied alpha
- Font drawing: Normal font and anti-aliasing font

Audio CODEC

- Supports AAC codec decoding
- Wavetable synthesis with up to 64 tones
- Advanced wavetable synthesizer capable of generating simulated stereo
- Wavetable including GM full set of 128 instruments and 47 sets of percussions
- PCM playback and record
- Digital audio playback

Audio interface and audio front-end

- Supports I2S interface
- High-resolution D/A converters for stereo audio playback
- Voice band A/D converter support
- Stereo to mono conversion

1.6 Bluetooth Features

Radio features

- Fully compliant with Bluetooth specification 4.0
- Low out-of-band spurious emissions support simultan eous operation with GPS and GSM/GPRS (2G) worldwide radio systems
- Low-IF architecture with high degree of linearity and high order channel filter
- Integrated T/R switch and Balun
- Fully integrated PA provides 7.5dBm output power
- -95dBm sensitivity with excellent interference rejection performance
- Hardware AGC dynamically adjusts receiver performance in changing environments

Baseband features

- Up to 4 simultaneous active ACL links
- Up to 4 simultaneous active BLE links
- Up to 1 simultaneous SCO or eSCO link with CVSD coding
- Supports eSCO
- BT Scatternet support: Up to 4 piconets simultaneously with background inquiry/page scan
- Supports sniff mode
- AFH and PTA collaborative support for WLAN/BT coexistence
- Idle mode and sleep mode enables ultra-low power consumption.
- Supports PCM interface and built-in programmable transcoders for linear voice with re-transmission
- Built-in hardware modem engine for access code correlation, header error correction, forward error correction, CRC, whitening and encryption
- Channel quality driven data rate adaptation
- Channel assessment for AFH

Platform features

- Embedded processor for Bluetooth protocol stack with built-in memory system
- Fully verified ROM based system with code patch for feature enhancement

1.7 FM Features

- 65-108MHz worldwide FM bands with 50KHz tuning step
- Supports RDS/RBDS radio data system
- Digital stereo demodulator
- Adaptive FM demodulator for both high- and low-quality scenarios
- Low sensitivity level with superior interference rejection
- Programmable de-emphasis (bypass/50 □S/75□S)
- Stereophonic multiplex signal (MPX) signal detection and demodulation
- Superior stereo noise reduction and soft mute volume control
- Audio dynamic range control
- Mono/stereo blending
- Audio sensitivity3dBμVemf (SINAD=26dB)
- Audio SINAD≥60dB
- Supports Anti-jamming algorithm
- Supports short antenna

1.8 General Descriptions

Figure 3 is the block diagram of MT2502A. Based on a multi-processor architecture, MT2502A integrates an ARM7EJ-S™ core, the main processor running high-level GSM protocol software as well as multimedia applications, single digital signal processor core, which manages the low-level MODEM and advanced audio functions, an embedded processor running Bluetooth baseband and link control protocol and the Bluetooth radio control.

MT2502A consists of the following subsystems:

- Microcontroller Unit (MCU) subsystem: Includes an ARM7EJ-S™ RISC processor and its accompanying memory management and interrupt handling logics
- Digital Signal Processor (DSP) subsystem: Includes a DSP and its accompanying memory, memory controller and interrupt controller
- MCU/DSP interface: Junction at which the MCU and the DSP exchange hardware and software information
- Microcontroller peripherals: Include all user interface modules and RF control interface modules
- Microcontroller coprocessors: Run computing-intensive processes in place of the microcontroller
- DSP peripherals: Hardware accelerators for GSM/GPRS (2G) channel codec
- Multimedia subsystem: Integrates several advanced accelerators to support multimedia applications
- Voice front-end: Data path for converting analog speech to and from digital speech
- Audio front-end: Data path for converting stereo audio from an audio source
- Baseband front-end: Data path for converting a digital signal to and from an analog signal from the RF modules
- Timing generator: Generates the control signals related to the TDMA frame timing
- Power, reset and clock subsystem: Manage the power, reset and clock distribution inside MT2502A.
- Bluetooth subsystem: Includes an embedded processor with embedded ROM/RAM system, baseband processor, and a high-performance radio block
- Power management unit: Self-contained power supply source which also controls the charging and system startup circuitry.

Details of the individual subsystems and blocks are described in the following chapters.

2 Product Descriptions

2.1 Pin Description

2.1.1 Ball Diagram

For MT2502A, a TFBGA 5.4mm*6.2mm, 143-ball, 0.4mm pitch package is offered. Pin-outs and the top view are illustrated in Figure 3 for this package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	RXLB	AVSS_2GHF	EINT		FREF	BT_LNA		AVSS_2GHF	BPI_BUS1		VDDK	BPI_BUS2	CMCSD0	A
B	RXHB	TX_LB	SRCLKENAI	XTAL1	XTAL2	AVSS_2GHF	AVDD15_BTRF	VIO28	CMMCLK	CMRST	SCL28	KCOL1	CMPDN	B
C		TX_HB	GPIO_10	GPIO_11	AVSS_2GHF		SDA28	CMCSK			KROW2	KROW1		C
D	VRF	AVSS_2GHF	AVSS_2GHF	EXT_CLK_SEL	BPI_BUS0		KROW0	KCOL0		KCOL4	GPIO_2	KCOL3	GPIO_3	D
E	VBAT_VA	AVSS44_ALDO			CMCSD1	KCOL2	KROW3	UTXD1	URXD1			GPIO_1	KROW4	E
F		FM_ANT_P	VCAMA	TESTMODE	GND	GND	GND	GPIO_0	SFSOUT	SFSHOLD	VSF	SFSWP		F
G	VREF	AVSS_FM		PWRKEY	CHRLDO	GND	GND	SFSCK	LSCE_B			SFSIN	SFSCS0	G
H	BATSNS	ISENSE			BATON	GND	GND	GND	LSRSTB	RESETB		SIM2_SCLK	VSIM2	H
J		DRV	KPLED	VCDT	AVSS44_PMU	AVSS28_ABB	GND	GND	LSA0	LPTE	SIM2_SRST	SIM2_SIO		J
K	AVSS44_PMU	ISINK			ACCDET	GND	SIM1_SCLK	SIM1_SRST	VMC			MCCK	MCDA0	K
L	AVSS44_BOOST	AVSS44_BOOST	AVDD_SPK	AU_MICBIAS0		AUXIN4	VSIM1		SIM1_SIO	LSCK	LSDA	MCDA2	MCCM0	L
M		SPK_OUTN	AVSS_SPK			XOUT	XIN			VBAT_DIGITAL	GND	MCDA1		M
N	AU_HPR	SPK_OUTP	AU_HSP	AU_HSN	AU_VIN1_N	AU_VIN0_N	APC	RTC_XOSC32_ENB	AVSS44_DLDO	VIBR	USB11_DM	MCDA3	VIO18	N
P	AU_HPL	AVSS_SPK	VA		AU_VIN1_P	AU_VIN0_P		VRTC	VCORE		USB11_DP	VUSB	VIO18	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Figure 3. Ball diagram and top view

2.1.2 Pin Coordination

Table 1. Pin coordinates

Pin#	Net name	Pin#	Net name	Pin#	Net name
A1	RXLB	D5	BPI_BUS0	H6	GND
A11	VDDK	D7	KROW0	H7	GND
A12	BPI_BUS2	D8	KCOL0	H8	GND
A13	CMCSD0	E1	VBAT_VA	H9	LSRSTB
A2	AVSS_2GHF	E12	GPIO_1	J10	LPTE
A3	EINT	E13	KROW4	J11	SIM2_SRST
A5	FREF	E2	AVSS44_ALDO	J12	SIM2_SIO
A6	BT_LNA	E5	CMCSD1	J2	DRV
A8	AVSS_2GHF	E6	KCOL2	J3	KPLED
A9	BPI_BUS1	E7	KROW3	J4	VCDT
B1	RXHB	E8	UTXD1	J5	AVSS44_PMU
B10	CMRST	E9	URXD1	J6	AVSS28_ABB
B11	SCL28	F10	SFSHOLD	J7	GND
B12	KCOL1	F11	VSF	J8	GND
B13	CMPDN	F12	SFSWP	J9	LSA0
B2	TX_LB	F2	FM_ANT_P	K1	AVSS44_PMU
B3	SRCLKENAI	F3	VCAMA	K12	MCCK
B4	XTAL1	F4	TESTMODE	K13	MCDA0
B5	XTAL2	F5	GND	K2	ISINK
B6	AVSS_2GHF	F6	GND	K5	ACCDET
B7	AVDD15_BTRF	F7	GND	K6	GND
B8	VIO28	F8	GPIO_0	K7	SIM1_SCLK
B9	CMMCLK	F9	SFSOUT	K8	SIM1_SRST
C11	KROW2	G1	VREF	K9	VMC
C12	KROW1	G12	SFSIN	L1	AVSS44_BOOST
C2	TX_HB	G13	SFSCS0	L10	LSCK
C3	GPIO_10	G2	AVSS_FM	L11	LSDA
C4	GPIO_11	G4	PWRKEY	L12	MCDA2
C5	AVSS_2GHF	G5	CHRLDO	L13	MCCM0
C7	SDA28	G6	GND	L2	AVSS44_BOOST
C8	CMCSK	G7	GND	L3	AVDD_SPK
D1	VRF	G8	SFSCK	L4	AU_MICBIAS0
D10	KCOL4	G9	LSCE_B	L6	AUXIN4
D11	GPIO_2	H1	BATSNS	L7	VSIM1
D12	KCOL3	H10	RESETB	L9	SIM1_SIO
D13	GPIO_3	H12	SIM2_SCLK	M10	VBAT_DIGITAL
D2	AVSS_2GHF	H13	VSIM2	M11	GND
D3	AVSS_2GHF	H2	ISENSE	M12	MCDA1
D4	EXT_CLK_SEL	H5	BATON	M2	SPK_OUTN

Pin#	Net name	Pin#	Net name	Pin#	Net name
M3	AVSS_SPK	N4	AU_HSN	P2	AVSS_SPK
M6	XOUT	N5	AU_VIN1_N	P3	VA
M7	XIN	N6	AU_VIN0_N	P5	AU_VIN1_P
N1	AU_HPR	N7	APC	P6	AU_VIN0_P
N10	VIBR	N8	RTC_XOSC32_ENB	P8	VRTC
N11	USB11_DM	N9	AVSS44_DLDO	P9	VCORE
N12	MCDA3	P1	AU_HPL		
N13	VIO18	P11	USB11_DP		
N2	SPK_OUTP	P12	VUSB		
N3	AU_HSP	P13	VIO18		

2.1.3 Detailed Pin Description

Table 2. Acronym for pin types

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output
DIO	Digital bi-direction
P	Power
G	Ground

Table 3. PIN function description and power domain

Pin name	Type	Description	Power domain
System			
RESETB	DIO	System reset	DVDD18_EMI
SRCLKENAI	DIO	26MHz clock request by external devices	VRF
EINT	DIO	External Interrupt	VRF
GPIO_0	DIO	General purpose input /output 0	DVDD28
GPIO_1	DIO	General purpose input /output 1	DVDD28
GPIO_2	DIO	General purpose input /output 2	DVDD28
GPIO_3	DIO	General purpose input /output 3	DVDD28
GPIO_10	DIO	General purpose input /output 10	VRF
GPIO_11	DIO	General purpose input /output 11	VRF

Pin name	Type	Description	Power domain
RF control circuitro			
BPI_BUS0	DIO	RF hard-wire control bus bit 0	DVDD28
BPI_BUS1	DIO	RF hard-wire control bus bit 1	DVDD28
BPI_BUS2	DIO	RF hard-wire control bus bit 2	DVDD28
UART interface			
URXD1	DIO	UART1 receive data	DVDD28
UTXD1	DIO	UART1 transmit data	DVDD28
Keypad interface			
KCOL0	DIO	Keypad column 0	DVDD28
KCOL1	DIO	Keypad column 1	DVDD28
KCOL2	DIO	Keypad column 2	DVDD28
KCOL3	DIO	Keypad column 3	DVDD28
KCOL4	DIO	Keypad column 4	DVDD28
KROW0	DIO	Keypad row 0	DVDD28
KROW1	DIO	Keypad row 1	DVDD28
KROW2	DIO	Keypad row 2	DVDD28
KROW3	DIO	Keypad row 3	DVDD28
KROW4	DIO	Keypad row 4	DVDD28
Camera interface			
CMRST	DIO	CMOS sensor reset signal output	DVDD28
CMPDN	DIO	CMOS sensor power down control	DVDD28
CMCSD0	DIO	CMOS sensor data input 0	DVDD28
CMCSD1	DIO	CMOS sensor data input 1	DVDD28
CMMCLK	DIO	CMOS sensor pixel clock input	DVDD28
CMCSK	DIO	CMOS sensor pixel clock output	DVDD28
MS/SD card interface			
MCDA0	DIO	SD serial data IO 0/memory stick serial data IO	DVDD33_MSDC
MCDA1	DIO	SD serial data IO 1/memory stick serial data IO	DVDD33_MSDC
MCDA2	DIO	SD serial data IO 2/memory stick serial data IO	DVDD33_MSDC
MCDA3	DIO	SD serial data IO 3/memory stick serial data IO	DVDD33_MSDC
MCCK	DIO	SD serial clock/memory stick serial clock	DVDD33_MSDC
MCCM0	DIO	SD command output/memory stick bus state output	DVDD33_MSDC
SIM card interface			
SIM1_SIO	DIO	SIM1 data input/outputs	VSIM1
SIM1_SRST	DIO	SIM1 card reset output	VSIM1
SIM1_SCLK	DIO	SIM1 card clock output	VSIM1
SIM2_SIO	DIO	SIM2 data input/outputs	VSIM2
SIM2_SRST	DIO	SIM2 card reset output	VSIM2
SIM2_SCLK	DIO	SIM2 card clock output	VSIM2

Pin name	Type	Description	Power domain
I2C interface			
SCL28	DIO	I2C clock 2.8v power domain	DVDD28
SDA28	DIO	I2C data 2.8v power domain	DVDD28
LCD interface			
LSRSTB	DIO	Serial display interface reset signal	DVDD18_EMI
LSCE_B	DIO	Serial display interface chip select output	DVDD18_EMI
LSCK	DIO	Serial display interface clock	DVDD18_EMI
LSDA	DIO	Serial display interface data	DVDD18_EMI
LSA0	DIO	Serial display interface address	DVDD18_EMI
LPTE	DIO	Serial display tearing signal	DVDD18_EMI
Serial Flash Interface			
SFCS0	DIO	Serial Flash chip select 0	DVDD28_SF
SFSIN	DIO	Serial Flash data input	DVDD28_SF
SFSOUT	DIO	Serial Flash data output	DVDD28_SF
SFSHOLD	DIO	Serial Flash data hold	DVDD28_SF
SFSWP	DIO	Serial Flash write protect	DVDD28_SF
SFSCK	DIO	Serial Flash clock	DVDD28_SF
FM			
FM_ANT_P	AI	FM input from antenna	VCAMA
Bluetooth			
BT_LNA	AIO	Bluetooth RF single-ended input	DVDD28
2G RF			
RXHB	AI	RF input for highband Rx (DCS/PCS)	VRF
RXLB	AI	RF input for lowband Rx (GSM900/GSM850)	VRF
TX_HB	AO	RF output for highband Tx (DCS/PCS)	VRF
TX_LB	AO	RF output pin for lowband Tx (GSM900/GSM850)	VRF
FREF	AO	DCXO reference clock output	VRF
XTAL1	AIO	Input 1 for DCXO crystal	VRF
XTAL2	AIO	Input 2 for DCXO crystal	VRF
EXT_CLK_SEL	AIO	DCXO mode selection	VRF
USB			
USB11_DM	AIO	D- data input/output	-
USB11_DP	AIO	D+ data input/output	-

Pin name	Type	Description	Power domain
Analog baseband			
AU_HPR	AIO	Audio head phone output (R channel)	AVDD28_ABB
AU_HPL	AIO	Audio head phone output (L channel)	AVDD28_ABB
AU_HSP	AIO	Voice handset output (positive)	AVDD28_ABB
AU_HSN	AIO	Voice handset output (negative)	AVDD28_ABB
AU_VIN0_P	AIO	Microphone 0 input (positive)	AVDD28_ABB
AU_VIN0_N	AIO	Microphone 0 input (negative)	AVDD28_ABB
AU_VIN1_P	AIO	Microphone 1 input (positive)	AVDD28_ABB
AU_VIN1_N	AIO	Microphone 1 input (negative)	AVDD28_ABB
AUX_IN4	AIO	Auxiliary ADC input	AVDD28_ABB
SPK_OUTP	AIO	Speaker positive output	VBAT_SPK
SPK_OUTN	AIO	Speaker negative output	VBAT_SPK
APC	AIO	Automatic power control DAC output	AVDD28_ABB
AU_MICBIAS0	AIO	Microphone bias source 0	AVDD28_ABB
ACCDET	AIO	Accessory detection	AVDD28_ABB
Real-time clock			
XIN	AIO	Input pin for 32K crystal	VRTC
XOUT	AIO	Input pin for 32K crystal	VRTC
RTC_XOSC32_ENB	DIO	Pin option for external 32K crystal	VRTC
Power management unit			
VA	AIO	LDO output for ABB - VA	VBAT_ANALOG
VCAMA	AIO	LDO output for sensor – VCAMA	VBAT_VA
VIBR	AIO	LDO output for vibrator - VIBR	VBAT_DIGITAL
VIO18	AIO	LDO output for 1.8V power - VIO18	VBAT_DIGITAL
VIO28	AIO	LDO output for 2.8V power - VIO28	VBAT_DIGITAL
VMC	AIO	LDO output for memory card - VMC	VBAT_DIGITAL
VSF	AIO	LDO output - VSF	VBAT_DIGITAL
VRF	AIO	LDO output for GSMRF - VRF	VBAT_VA
VRTC	AIO	LDO output for RTC - VRTC	VBAT_DIGITAL
VSIM1	AIO	LDO output for 1st SIM - VSIM	VBAT_DIGITAL
VSIM2	AIO	LDO output for 2nd SIM - VSIM2	VBAT_DIGITAL
VUSB	AIO	LDO output for USB - VUSB	VBAT_DIGITAL
VCORE	AIO	LDO output for core circuit - Vcore	VBAT_DIGITAL
VREF	AIO	Band gap reference	BATSNS
VCDT	AIO	Charger-In level sense pin	BATSNS
DRV	AIO	IDAC current output open-drain pin	BATSNS
BATON	AIO	Battery Pack, NTC connected pin	BATSNS
ISENSE	AIO	Top node of current sensing 0.2ohm Rsense resistor	BATSNS
CHRLDO	AIO	2.8V shunt-regulator output	BATSNS
ISINK0	AIO	Backlight driver channel 0	VBAT_VA

Pin name	Type	Description	Power domain
KPLED	AIO	Keypad led driver	VBAT_VA
TESTMODE	AIO	Test mode	BATSNS
PWRKEY	AIO	PWR key	BATSNS
AVDD25_V2P5	AIO	Reference voltage for ABT	-
Analog power			
AVDD15_BTRF	P	BTRF power input	-
VBAT_DIGITAL	P	Digital LDOs used battery voltage input	-
VBAT_VA	P	Analog LDOs used battery voltage input	-
AVDD_SPK	P	Input for loud speaker driver	-
BATSNS	P	Battery node of battery pack	-
Analog ground			
AVSS28_ABB	G	ABB 2.8V ground	-
AVSS_2G	G	2G RF ground	-
AVSS_FM	G	FM ground	-
AVSS44_PMU	G	PMU ground	-
AVSS44_ALDO	G	ALDO ground	-
AVSS44_DLDO	G	DLDO ground	-
AVSS_SPK	G	SPK ground	-
AGND	G	GND for VREF	-
AVSS44_BOOST	G	Audio boost GND	-
Digital power			
VDDK	P	Core power	-
Digital ground			
GND	G	Ground	-

Table 4. Acronym for state of pins

Abbreviation	Description
I	Input
LO	Low output
HO	High output
LO	Low output
PU	Pull-up
PD	Pull-down
-	No PU/PD
0~N	Aux. function number
X	Delicate function pin

Table 5. State of pins

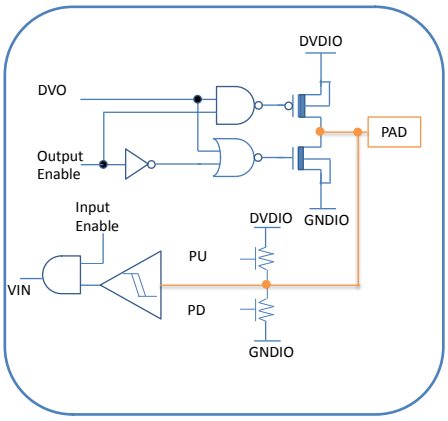
Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
System						
RESETB	HO	1	-	DIOH3/DIOL3	No need	IO Type 3
SRCLKENAI	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
EINT	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
GPIO_0	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
GPIO_1	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
GPIO_2	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
GPIO_3	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
GPIO_10	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
GPIO_11	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
RF control circuitry						
BPI_BUS0	LO	1	PD	DIOH2/DIOL2	No need	IO Type 2
BPI_BUS1	I	1	PD	DIOH2/DIOL2	No need	IO Type 2
BPI_BUS2	I	1	PD	DIOH2/DIOL2	No need	IO Type 2
UART interface						
URXD1	I	1	PU	DIOH3/DIOL3	No need	IO Type 3
UTXD1	HO	1	PU	DIOH2/DIOL2	No need	IO Type 2
Keypad Interface						
KCOL0	I	0	PU	DIOH4/DIOL4	No need	IO Type 4
KCOL1	I	0	PU	DIOH4/DIOL4	No need	IO Type 4
KCOL2	I	0	PU	DIOH4/DIOL4	No need	IO Type 4
KCOL3	I	0	PU	DIOH4/DIOL4	No need	IO Type 4
KCOL4	I	0	PU	DIOH4/DIOL4	No need	IO Type 4
KROW0	I	0	PD	DIOH5/DIOL5	No need	IO Type 5
KROW1	I	0	PD	DIOH5/DIOL5	No need	IO Type 5
KROW2	I	0	PD	DIOH5/DIOL5	No need	IO Type 5
KROW3	I	0	PD	DIOH5/DIOL5	No need	IO Type 5
KROW4	I	0	PD	DIOH5/DIOL5	No need	IO Type 5
Camera interface						
CMRST	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
CMPDN	HO	0	-	DIOH3/DIOL3	No need	IO Type 3
CMCSD0	I	0	PU	DIOH3/DIOL3	No need	IO Type 3
CMCSD1	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
CMMCLK	I	0	PD	DIOH3/DIOL3	No need	IO Type 3

[1] The column “State” of “Reset” shows the pin state during reset. (Input, High Output, Low Output, etc)

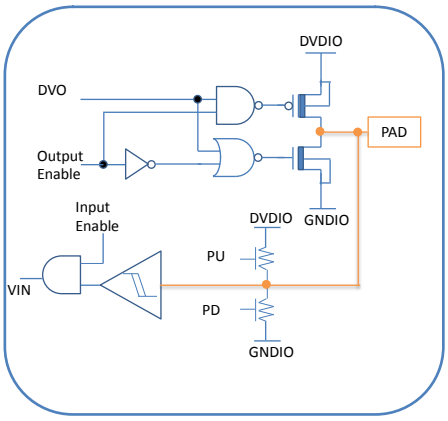
[2] The column “Aux” for “Reset” means the default aux function number, shown in the table “Pin Multiplexing, Capability and Settings”.

[3] The column “PU/PD” for “Reset” means if there is internal pull-up or pull-down when the pin is input in the reset state.

Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
CMCSK	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
MS/SD card interface						
MCDA0	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
MCDA1	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
MCDA2	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
MCDA3	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
MCCK	I	0	PU	DIOH3/DIOL3	No need	IO Type 3
MCCM0	I	0	PU	DIOH3/DIOL3	No need	IO Type 3
SIM card interface						
SIM1_SIO	I	1	PD	DIOH6/DIOL6	No need	IO Type 6
SIM1_SRST	I	1	PD	DIOH6/DIOL6	No need	IO Type 6
SIM1_SCLK	I	1	PD	DIOH6/DIOL6	No need	IO Type 6
SIM2_SIO	I	1	PD	DIOH6/DIOL6	No need	IO Type 6
SIM2_SRST	I	1	PD	DIOH6/DIOL6	No need	IO Type 6
SIM2_SCLK	I	1	PD	DIOH6/DIOL6	No need	IO Type 6
I2C interface						
SCL28	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
SDA28	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
LCD interface						
LSRSTB	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
LSCE_B	HO	1	-	DIOH3/DIOL3	No need	IO Type 3
LSCK	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
LSDA	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
LSA0	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
LPTE	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
Serial Flash Interface						
SFCS0	HO	1	-	DIOH7/DIOL7	No need	IO Type 7
SFSIN	I	1	PU	DIOH7/DIOL7	No need	IO Type 7
SFSOUT	HO	1	-	DIOH7/DIOL7	No need	IO Type 7
SFSHOLD	HO	1	-	DIOH7/DIOL7	No need	IO Type 7
SFSWP	HO	1	-	DIOH7/DIOL7	No need	IO Type 7
SFSCK	LO	1	-	DIOH7/DIOL7	No need	IO Type 7



IO type1



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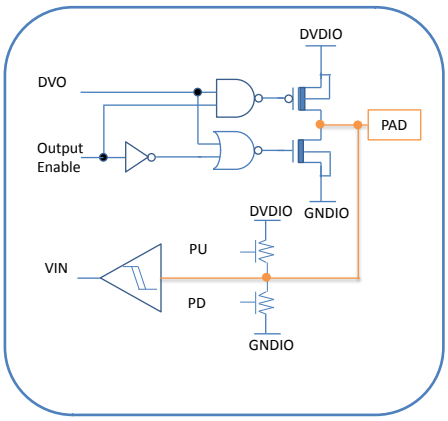

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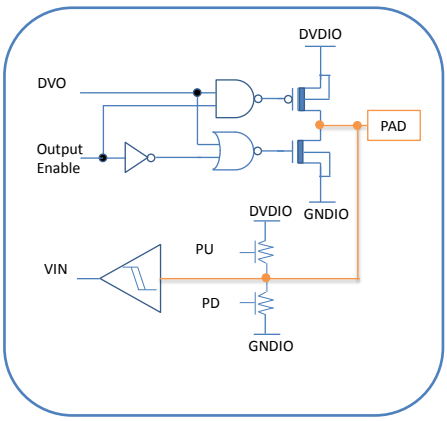

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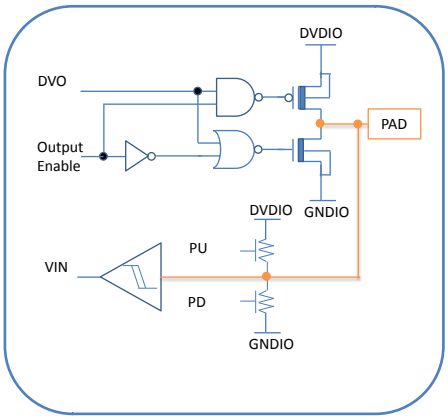
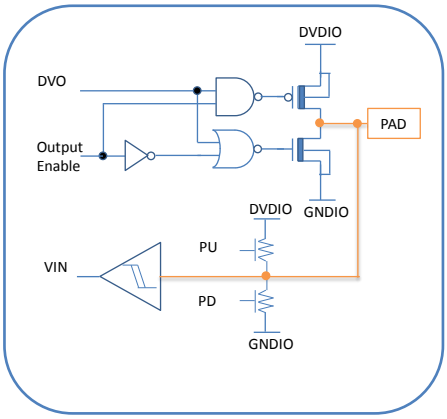
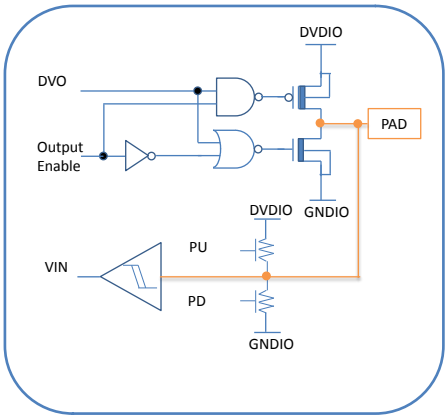


IO type5



IO type6



IO type7

Figure 4. IO types in state of pins

2.1.4 Pin Multiplexing, Capability and Settings

Table 6. Acronym for pull-up and pull-down types

Abbreviation	Description
PU	Pull-up, not controllable
PD	Pull-down, not controllable
CU	Pull-up, controllable
CD	Pull-down, controllable
X	Cannot pull-up or pull-down

Table 7. Capability of PU/PD, driving and Schmitt trigger

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
GPIO_0	0	GPIO0	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT0	I	CU, CD	4, 8, 12, 16mA	0
	2	XP	AIO	-	4, 8, 12, 16mA	0
	3	U3RXD	I	CU, CD	4, 8, 12, 16mA	0
	4	CMCSD2	I	CU, CD	4, 8, 12, 16mA	0
	5	CMCSK	I	CU, CD	4, 8, 12, 16mA	0
	6	EDIDO	O	CU, CD	4, 8, 12, 16mA	0
	7	JTDI	I	PU	4, 8, 12, 16mA	0
	8	BTJTDI	I	CU, CD	4, 8, 12, 16mA	0
	9	FMJTDI	I	CU, CD	4, 8, 12, 16mA	0
GPIO_1	0	GPIO1	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT1	I	CU, CD	4, 8, 12, 16mA	0
	2	XM	AIO	-	4, 8, 12, 16mA	0
	3	U3TXD	O	CU, CD	4, 8, 12, 16mA	0
	4	U1CTS	I	CU, CD	4, 8, 12, 16mA	0
	5	CMMCLK	O	CU, CD	4, 8, 12, 16mA	0
	6	EDIDI	I	CU, CD	4, 8, 12, 16mA	0
	7	JTMS	I	PU	4, 8, 12, 16mA	0
	8	BTJTMS	I	CU, CD	4, 8, 12, 16mA	0
	9	FMJTMS	I	CU, CD	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
GPIO_2	0	GPIO2	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT2	O	CU, CD	4, 8, 12, 16mA	0
	2	YP	AIO	-	4, 8, 12, 16mA	0
	3	GPSFSYNC	O	CU, CD	4, 8, 12, 16mA	0
	4	PWM0	O	CU, CD	4, 8, 12, 16mA	0
	5	CMCSD0	I	CU, CD	4, 8, 12, 16mA	0
	6	EDIWS	O	CU, CD	4, 8, 12, 16mA	0
	7	JTRST_B	I	PD	4, 8, 12, 16mA	0
	8	BTJTRSTB	I	CU, CD	4, 8, 12, 16mA	0
	9	FMJTRSTB	I	CU, CD	4, 8, 12, 16mA	0
GPIO_3	0	GPIO3	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCINS	I	CU, CD	4, 8, 12, 16mA	0
	2	YM	AIO	-	4, 8, 12, 16mA	0
	4	PWM1	O	CU, CD	4, 8, 12, 16mA	0
	5	CMCSD1	I	CU, CD	4, 8, 12, 16mA	0
	6	EDICK	O	CU, CD	4, 8, 12, 16mA	0
	7	JTDO	O	CU, CD	4, 8, 12, 16mA	0
	8	BTJTDO	O	CU, CD	4, 8, 12, 16mA	0
	9	FMJTDO	O	CU, CD	4, 8, 12, 16mA	0
URXD1	0	GPIO10	IO	CU, CD	4, 8, 12, 16mA	0
	1	U1RXD	I	PU	4, 8, 12, 16mA	0
	2	CMRST	O	CU, CD	4, 8, 12, 16mA	0
	3	EINT9	I	CU, CD	4, 8, 12, 16mA	0
	4	MCINS	I	CU, CD	4, 8, 12, 16mA	0
UTXD1	0	GPIO11	IO	CU, CD	4, 8, 12, 16mA	0
	1	U1TXD	O	CU, CD	4, 8, 12, 16mA	0
	2	CMPDN	O	CU, CD	4, 8, 12, 16mA	0
	3	EINT10	I	CU, CD	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
KCOL4	0	GPIO12	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL4	IO	-	4, 8, 12, 16mA	0
	2	U2RXD	I	CU, CD	4, 8, 12, 16mA	0
	3	EDIDI	I	CU, CD	4, 8, 12, 16mA	0
	4	FMJTDI	I	CU, CD	4, 8, 12, 16mA	0
	5	JTDI	I	PU	4, 8, 12, 16mA	0
	6	BTJTDI	I	CU, CD	4, 8, 12, 16mA	0
KCOL3	0	GPIO13	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL3	IO	-	4, 8, 12, 16mA	0
	2	EINT11	I	CU, CD	4, 8, 12, 16mA	0
	3	PWM0	O	CU, CD	4, 8, 12, 16mA	0
	4	FMJTMS	I	CU, CD	4, 8, 12, 16mA	0
	5	JTMS	I	PU	4, 8, 12, 16mA	0
	6	BTJTMS	I	CU, CD	4, 8, 12, 16mA	0
KCOL2	0	GPIO14	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL2	IO	-	4, 8, 12, 16mA	0
	2	EINT12	I	CU, CD	4, 8, 12, 16mA	0
	3	U1RTS	I	CU, CD	4, 8, 12, 16mA	0
KCOL1	0	GPIO15	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL1	IO	-	4, 8, 12, 16mA	0
	2	GPSFSYNC	O	CU, CD	4, 8, 12, 16mA	0
	3	U1CTS	I	CU, CD	4, 8, 12, 16mA	0
	4	FMJTCK	I	CU, CD	4, 8, 12, 16mA	0
	5	JTCK	I	PU	4, 8, 12, 16mA	0
	6	BTJTCK	I	CU, CD	4, 8, 12, 16mA	0
KCOL0	0	GPIO16	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL0	IO	-	4, 8, 12, 16mA	0
KROW4	0	GPIO17	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW4	IO	-	4, 8, 12, 16mA	0
	2	U2TXD	O	CU, CD	4, 8, 12, 16mA	0
	3	EDICK	O	CU, CD	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
KROW3	0	GPIO18	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW3	IO	-	4, 8, 12, 16mA	0
	2	EINT13	I	CU, CD	4, 8, 12, 16mA	0
	3	CLKO0	O	CU, CD	4, 8, 12, 16mA	0
	4	FMJTRSTB	I	CU, CD	4, 8, 12, 16mA	0
	5	JTRST_B	I	PD	4, 8, 12, 16mA	0
	6	BTJTRSTB	I	CU, CD	4, 8, 12, 16mA	0
KROW2	0	GPIO19	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW2	IO	-	4, 8, 12, 16mA	0
	2	PWM1	O	CU, CD	4, 8, 12, 16mA	0
	3	EDIWS	O	CU, CD	4, 8, 12, 16mA	0
	4	FMJTDO	O	CU, CD	4, 8, 12, 16mA	0
	5	JTDO	O	CU, CD	4, 8, 12, 16mA	0
	6	BTJTDO	O	CU, CD	4, 8, 12, 16mA	0
KROW1	0	GPIO20	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW1	IO	-	4, 8, 12, 16mA	0
	2	EINT14	I	CU, CD	4, 8, 12, 16mA	0
	3	EDIDO	O	CU, CD	4, 8, 12, 16mA	0
	4	BTPRI	IO	CU, CD	4, 8, 12, 16mA	0
	5	JTRCK	O	CU, CD	4, 8, 12, 16mA	0
	6	BTDBGACKN	O	CU, CD	4, 8, 12, 16mA	0
KROW0	0	GPIO21	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW0	IO	-	4, 8, 12, 16mA	0
	5	MCINS	I	CU, CD	4, 8, 12, 16mA	0
	6	BTDBGIN	I	CU, CD	4, 8, 12, 16mA	0
BPI_BUS2	0	GPIO22	IO	CU, CD	4, 8, 12, 16mA	0
	1	BPI_BUS2	O	CU, CD	4, 8, 12, 16mA	0
BPI_BUS1	0	GPIO23	IO	CU, CD	4, 8, 12, 16mA	0
	1	BPI_BUS1	O	CU, CD	4, 8, 12, 16mA	0
BPI_BUS0	0	GPIO24	IO	CU, CD	4, 8, 12, 16mA	0
	1	BPI_BUS0	IO	CU, CD	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
CMRST	0	GPIO25	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMRST	O	CU, CD	4, 8, 12, 16mA	0
	2	LSRSTB	O	CU, CD	4, 8, 12, 16mA	0
	3	CLKO1	O	CU, CD	4, 8, 12, 16mA	0
	4	EINT15	I	CU, CD	4, 8, 12, 16mA	0
	5	FMJTDI	I	CU, CD	4, 8, 12, 16mA	0
	6	JTDI	I	PU	4, 8, 12, 16mA	0
CMPDN	0	GPIO26	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMPDN	O	CU, CD	4, 8, 12, 16mA	0
	2	LSCK1	O	CU, CD	4, 8, 12, 16mA	0
	3	DAICLK	O	CU, CD	4, 8, 12, 16mA	0
	4	SPICS	IO	CU, CD	4, 8, 12, 16mA	0
	5	FMJTMS	I	CU, CD	4, 8, 12, 16mA	0
	6	JTMS	I	PU	4, 8, 12, 16mA	0
CMCSD0	0	GPIO27	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMCSD0	I	CU, CD	4, 8, 12, 16mA	0
	2	LSCE_B1	O	CU, CD	4, 8, 12, 16mA	0
	3	DAIPCMIN	I	CU, CD	4, 8, 12, 16mA	0
	4	SPISCK	IO	CU, CD	4, 8, 12, 16mA	0
	5	FMJTCK	I	CU, CD	4, 8, 12, 16mA	0
	6	JTCK	I	PU	4, 8, 12, 16mA	0
	8	MC2CM0	O	-	4, 8, 12, 16mA	0
CMCSD1	0	GPIO28	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMCSD1	I	CU, CD	4, 8, 12, 16mA	0
	2	LSDA1	IO	CU, CD	4, 8, 12, 16mA	0
	3	DAIPCMOUT	O	CU, CD	4, 8, 12, 16mA	0
	4	SPIMOSI	IO	CU, CD	4, 8, 12, 16mA	0
	5	FMJTRSTB	I	CU, CD	4, 8, 12, 16mA	0
	6	JTRST_B	I	PD	4, 8, 12, 16mA	0
	8	MC2CK	O	-	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
CMMCLK	0	GPIO29	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMMCLK	O	CU, CD	4, 8, 12, 16mA	0
	2	LSA0DA1	O	CU, CD	4, 8, 12, 16mA	0
	3	DAISYNC	O	CU, CD	4, 8, 12, 16mA	0
	4	SPIMISO	IO	CU, CD	4, 8, 12, 16mA	0
	5	FMJTDO	O	CU, CD	4, 8, 12, 16mA	0
	6	JTDO	O	CU, CD	4, 8, 12, 16mA	0
	8	MC2DA0	IO	-	4, 8, 12, 16mA	0
CMCSK	0	GPIO30	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMCSK	I	CU, CD	4, 8, 12, 16mA	0
	2	LPTE	I	CU, CD	4, 8, 12, 16mA	0
	3	CMCSD2	I	CU, CD	4, 8, 12, 16mA	0
	4	EINT16	I	CU, CD	4, 8, 12, 16mA	0
	6	JTRCK	O	CU, CD	4, 8, 12, 16mA	0
MCCK	0	GPIO31	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCCK	O	-	4, 8, 12, 16mA	0
	4	U2RXD	I	CU, CD	4, 8, 12, 16mA	0
MCCM0	0	GPIO32	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCCM0	IO	-	4, 8, 12, 16mA	0
	4	U2TXD	O	CU, CD	4, 8, 12, 16mA	0
MCDA0	0	GPIO33	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCDA0	IO	-	4, 8, 12, 16mA	0
	4	DAISYNC	O	CU, CD	4, 8, 12, 16mA	0
MCDA1	0	GPIO34	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCDA1	IO	-	4, 8, 12, 16mA	0
	2	EINT17	I	CU, CD	4, 8, 12, 16mA	0
	4	DAIPCMIN	I	CU, CD	4, 8, 12, 16mA	0
MCDA2	0	GPIO35	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCDA2	IO	-	4, 8, 12, 16mA	0
	2	EINT18	I	CU, CD	4, 8, 12, 16mA	0
	4	DAICLK	O	CU, CD	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
MCDA3	0	GPIO36	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCDA3	IO	-	4, 8, 12, 16mA	0
	2	EINT19	I	CU, CD	4, 8, 12, 16mA	0
	3	CLKO2	O	CU, CD	4, 8, 12, 16mA	0
	4	DAIPCMOUT	O	CU, CD	4, 8, 12, 16mA	0
SIM1_SIO	0	GPIO37	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIM1_SIO	IO	-	2, 4, 6, 8mA	0
SIM1_SRST	0	GPIO38	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIM1_SRST	IO	-	2, 4, 6, 8mA	0
SIM1_SCLK	0	GPIO39	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIM1_SCLK	IO	-	2, 4, 6, 8mA	0
SIM2_SIO	0	GPIO40	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIM2_SIO	IO	-	2, 4, 6, 8mA	0
	3	U2RTS	O	CU, CD	2, 4, 6, 8mA	0
SIM2_SRST	0	GPIO41	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIM2_SRST	IO	-	2, 4, 6, 8mA	0
	2	CLKO3	O	CU, CD	2, 4, 6, 8mA	0
	3	U2CTS	I	CU, CD	2, 4, 6, 8mA	0
SIM2_SCLK	0	GPIO42	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIM2_SCLK	IO	-	2, 4, 6, 8mA	0
	2	LSCE1_B1	O	CU, CD	2, 4, 6, 8mA	0
SCL	0	GPIO43	IO	CU, CD	4, 8, 12, 16mA	0
	1	SCL	IO	CU, CD	4, 8, 12, 16mA	0
SDA	0	GPIO44	IO	CU, CD	4, 8, 12, 16mA	0
	1	SDA	IO	CU, CD	4, 8, 12, 16mA	0
LSRSTB	0	GPIO45	IO	CU, CD	4, 8, 12, 16mA	0
	1	LSRSTB	O	CU, CD	4, 8, 12, 16mA	0
	3	CMRST	O	CU, CD	4, 8, 12, 16mA	0
LSCE_B0	0	GPIO46	IO	CU, CD	4, 8, 12, 16mA	0
	1	LSCE_B0	O	CU, CD	4, 8, 12, 16mA	0
	2	EINT20	I	CU, CD	4, 8, 12, 16mA	0
	3	CMCSD0	I	CU, CD	4, 8, 12, 16mA	0
	4	CLKO4	O	CU, CD	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
LSCK0	0	GPIO47	IO	CU, CD	4, 8, 12, 16mA	0
	1	LSCK0	O	CU, CD	4, 8, 12, 16mA	0
	3	CMPDN	O	CU, CD	4, 8, 12, 16mA	0
LSDA0	0	GPIO48	IO	CU, CD	4, 8, 12, 16mA	0
	1	LSDA0	IO	-	4, 8, 12, 16mA	0
	2	EINT21	I	CU, CD	4, 8, 12, 16mA	0
	3	CMCSD1	I	CU, CD	4, 8, 12, 16mA	0
	4	WIFITOBT	I	CU, CD	4, 8, 12, 16mA	0
LSA0	0	GPIO49	IO	CU, CD	4, 8, 12, 16mA	0
	1	LSA0DA0	O	-	4, 8, 12, 16mA	0
	2	LSCE1_B0	O	CU, CD	4, 8, 12, 16mA	0
	3	CMMCLK	O	CU, CD	4, 8, 12, 16mA	0
LPTE	0	GPIO50	IO	CU, CD	4, 8, 12, 16mA	0
	1	LPTE	I	CU, CD	4, 8, 12, 16mA	0
	2	EINT22	I	CU, CD	4, 8, 12, 16mA	0
	3	CMCSK	I	CU, CD	4, 8, 12, 16mA	0
	4	CMCSD2	I	CU, CD	4, 8, 12, 16mA	0
	6	MCINS	I	CU, CD	4, 8, 12, 16mA	0
	9	CLKO5	O	CU, CD	4, 8, 12, 16mA	0
RESETB	0	GPIO51	IO	CU, CD	4, 8, 12, 16mA	0
	1	RESETB	IO	CU, CD	4, 8, 12, 16mA	0
EINT	0	AGPI52	I	CU, CD	8mA	0
	2	EINT23	I	CU, CD	8mA	0
SRCLKENAI	0	AGPI53	I	CU, CD	8mA	0
	1	SRCLKENAI	I	CU, CD	8mA	0
	2	EINT24	I	-	8mA	0
GPIO_10	0	AGPIO54	IO	CU, CD	8mA	0
GPIO_11	0	AGPIO55	IO	CU, CD	8mA	0
SFCS0	1	SFCS0	O	CU, CD	2, 4, 6, 8, 10, 12, 14, 16mA	0
SFSIN	1	SFSIN	IO	CU, CD	2, 4, 6, 8, 10, 12, 14, 16mA	0
SFSOUT	1	SFSOUT	IO	CU, CD	2, 4, 6, 8, 10, 12, 14, 16mA	0
SFSHOLD	1	SFSHOLD	IO	CU, CD	2, 4, 6, 8, 10, 12, 14, 16mA	0
SFSWP	1	SFSWP	IO	CU, CD	2, 4, 6, 8, 10, 12, 14, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
SFSCK	1	SFSCK	O	CU, CD	2, 4, 6, 8, 10, 12, 14, 16mA	0

2.2 Electrical Characteristics

2.2.1 Absolute Maximum Ratings

Table 8. Absolute maximum ratings for power supply

Symbol or pin name	Description	Min.	Max.	Unit
VBAT_DIGITAL	Digital used battery voltage input	-0.3	+4.4	V
VBAT_VA	Analog used battery voltage input	-0.3	+4.4	V
AVDD_SPK	VBAT input for loud speaker driver	-0.3	+5.5	V
VDDK	1.3v core power	-0.3	+1.43	V

Table 9. Absolute maximum ratings for voltage input

Symbol or pin name	Description	Min.	Max.	Unit
VIN1	Digital input voltage for IO Type 1	-0.3	3.08	V
VIN2	Digital input voltage for IO Type 2	-0.3	3.08	V
VIN3	Digital input voltage for IO Type 3	-0.3	3.63	V
VIN4	Digital input voltage for IO Type 4	-0.3	3.08	V
VIN5	Digital input voltage for IO Type 5	-0.3	3.08	V
VIN6	Digital input voltage for IO Type 6	-0.3	3.08	V
VIN7	Digital input voltage for IO Type 7	-0.3	3.63	V

Table 10. Absolute maximum ratings for storage temperature

Symbol or pin name	Description	Min.	Max.	Unit
Tstg	Storage temperature	-55	125	°C

2.2.2 Recommended Operating Conditions

Table 11. Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
VBAT_DIGITAL	Digital used battery voltage input	3.4	3.8	4.2	V
VBAT_VA	Analog used battery voltage input	3.4	3.8	4.2	V
AVDD_SPK	VBAT input for loud speaker driver	3.4	3.8	4.2	V
VDDK	1.2v core power	1.17	1.3	1.43	V

Table 12. Recommended operating conditions for voltage input

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
VIN1	Digital input voltage for IO Type 1	-0.3	-	DVDIO+0.3	V
VIN2	Digital input voltage for IO Type 2	-0.3	-	DVDIO+0.3	V
VIN3	Digital input voltage for IO Type 3	-0.3	-	DVDIO+0.3	V
VIN4	Digital input voltage for IO Type 4	-0.3	-	DVDIO+0.3	V
VIN5	Digital input voltage for IO Type 5	-0.3	-	DVDIO+0.3	V
VIN6	Digital input voltage for IO Type 6	-0.3	-	DVDIO+0.3	V
VIN7	Digital input voltage for IO Type 7	-0.3	-	DVDIO+0.3	V

Table 13. Recommended operating conditions for operating temperature

Symbol or pin name	Description	Min.	Typ	Max.	Unit
Tc	Operating temperature	-20	-	85	°C

2.2.3 Electrical Characteristics under Recommended Operating Conditions

Table 14. Electrical characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DIIH1	Digital high input current for IO Type 1	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN1 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN1 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1<VIN1<3.1	6.1	-	82.5	
DIIL1	Digital low input current for IO Type 1	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN1 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN1 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN1 < 0.7	-12.5	-	22.5	
DIOH1	Digital high output current for IO Type 1	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
DIOL1	Digital low output current for IO Type 1	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DRPU1	Digital I/O pull-up resistance for IO Type 1	DVDIO = 2.8V	40	85	190	kΩ
DRPD1	Digital I/O pull-down resistance for IO Type 1	DVDIO = 2.8V	40	85	190	kΩ
DVOH1	Digital output high voltage for IO Type 1	DVDIO = 2.8V	2.38			V
DVOL1	Digital output low voltage for IO Type 1	DVDIO = 2.8V			0.42	V
DIIH2	Digital high input current for IO Type 2	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN1 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN1 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1<VIN1<3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN1 < 2.1	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN1 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN1 < 2.1	-0.8	-	35	
DIIL2	Digital low input current for IO Type 2	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN2 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN2 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN2 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN1 < 0.45	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN1 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN1 < 0.45	-9.3	-	11.4	

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DIOH2	Digital high output current for IO Type 2	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-12	-	-	mA
DIOL2	Digital low output current for IO Type 2	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA
DRPU2	Digital I/O pull-up resistance for IO Type 2	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPD2	Digital I/O pull-down resistance for IO Type 2	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DVOH2	Digital output high voltage for IO Type 2	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL2	Digital output low voltage for IO Type 2	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V
DIIH3	Digital high input current for IO Type 3	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN3 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN3 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1 < VIN3 < 3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN3 < 2.1	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN3 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN3 < 2.1	-0.8	-	35	

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DIIL3	Digital low input current for IO Type 3	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN3 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN3 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN3 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN3 < 0.45	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN3 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN3 < 0.45	-9.3	-	11.4	
DIOH3	Digital high output current for IO Type 3	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-12	-	-	mA
DIOL3	Digital low output current for IO Type 3	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA
DRPU3	Digital I/O pull-up resistance for IO Type 3	DVDIO = 2.8V	10	47	100	kΩ
		DVDIO = 1.8V	10	47	100	kΩ
DRPD3	Digital I/O pull-down resistance for IO Type 3	DVDIO = 1.8V	10	47	100	kΩ
		DVDIO = 2.8V	10	47	100	kΩ
DVOH3	Digital output high voltage for IO Type 3	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL3	Digital output low voltage for IO Type 3	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V
DIIH4	Digital high input current for IO Type 4	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN4 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN4 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1 < VIN4 < 3.1	6.1	-	82.5	

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DIIL4	Digital low input current for IO Type 4	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN4 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN4 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN4 < 0.7	-12.5	-	22.5	
DIOH4	Digital high output current for IO Type 4	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
DIOL4	Digital low output current for IO Type 4	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
DRPU4	Digital I/O pull-up resistance for IO Type 4 (GPIO mode)	DVDIO = 2.8V	15	36	55	kΩ
DRPD4	Digital I/O pull-down resistance for IO Type 4 (GPIO mode)	DVDIO = 2.8V	15	36	55	kΩ
DRPU4 1200K	Digital I/O pull-up resistance for IO Type 4 (Key PAD mode)	DVDIO = 2.8V	1200	-	-	kΩ
DRPD4 1200K	Digital I/O pull-down resistance for IO Type 4 (Key PAD mode)	DVDIO = 2.8V	1200	-	-	kΩ
DVOH4	Digital output high voltage for IO Type 4	DVDIO = 2.8V	2.38			V
DVOL4	Digital output low voltage for IO Type 4	DVDIO = 2.8V			0.42	V
DIIH5	Digital high input current for IO Type 5	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN5 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN5 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1 < VIN5 < 3.1	6.1	-	82.5	
DIIL5	Digital low input current for IO Type 5	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN5 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN5 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN5 < 0.7	-12.5	-	22.5	

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DIOH5	Digital high output current for IO Type 5	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
DIOL5	Digital low output current for IO Type 5	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
DRPU5	Digital I/O pull-up resistance for IO Type 5 (GPIO mode)	DVDIO = 2.8V	15	36	55	kΩ
DRPD5	Digital I/O pull-down resistance for IO Type 5 (GPIO mode)	DVDIO = 2.8V	15	36	55	kΩ
DRPU5 1K	Digital I/O pull-up resistance for IO Type 4 (Key PAD mode)	DVDIO = 2.8V	1	-	-	kΩ
DRPD5 1K	Digital I/O pull-down resistance for IO Type 4 (Key PAD mode)	DVDIO = 2.8V	1	-	-	kΩ
DVOH5	Digital output high voltage for IO Type 5	DVDIO = 2.8V	2.38			V
DVOL5	Digital output low voltage for IO Type 5	DVDIO = 2.8V			0.42	V
DIIH6	Digital high input current for IO Type 6	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN6 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN6 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1 < VIN6 < 3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN6 < 2.1	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN6 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN6 < 2.1	-0.8	-	35	

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DIIL6	Digital low input current for IO Type 6	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN6 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN6 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN6 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN6 < 0.45	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN6 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN6 < 0.45	-9.3	-	11.4	
DIOH6	Digital high output current for IO Type 6	DVOH > 2.38V, DVDIO = 2.8V	-8	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-6	-	-	mA
DIOL6	Digital low output current for IO Type 6	DVOL < 0.42V, DVDIO = 2.8V	-	-	8	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	6	mA
DRPU6	Digital I/O pull-up resistance for IO Type 6	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPD6	Digital I/O pull-down resistance for IO Type 6	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DVOH6	Digital output high voltage for IO Type 6	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL6	Digital output low voltage for IO Type 6	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DIIH7	Digital high input current for IO Type 7	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN7 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN7 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1<VIN7<3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN7 < 2.1	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN7 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN7 < 2.1	-0.8	-	35	
DIIL7	Digital low input current for IO Type 7	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN7 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN7 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN7 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN7 < 0.45	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN7 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN7 < 0.45	-5	-	5	
DIOH7	Digital high output current for IO Type 7	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-12	-	-	mA
DIOL7	Digital low output current for IO Type 7	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA
DRPU7	Digital I/O pull-up	DVDIO = 2.8V	40	85	190	kΩ

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	resistance for IO Type 7	DVDIO = 1.8V	70	150	320	kΩ
DRPD7	Digital I/O pull-down resistance for IO Type 7	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DVOH7	Digital output high voltage for IO Type 7	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL7	Digital output low voltage for IO Type 7	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V

2.3 System Configuration

2.3.1 Strapping Resistors

Table 15. Strapping table

Pin name	Description	Trapping condition
LSA0	Pull-up with 10K resister(Default internal pull-down with 47K resister)	Power-on reset
BPI_BUS1	Pull-up with 10K resister (Default internal pull-down with 75K resister)	Power-on reset
BPI_BUS2	Pull-up with 10K resister (Default internal pull-down with 75K resister)	Power-on reset

2.3.2 Mode Selection

Table 16. Mode selection of chip

Pin name	Description
EXT_CLK_SEL	GND: Uses DCXO as 26M clock source VRF: Uses external clock as 26M clock source
RTC_XOSC32_ENB	GND: Uses external 32K crystal as RTC clock source VRTC: Uses internal 32K as RTC clock source
LSA0	GND: Uses 1.8V serial flash device DVDD18_EMI: Uses 3.3V serial flash device
KCOL0	GND: Boots ROM to enter USB download mode DVDD28: Normal boot-up mode
{BPI_BUS1,BPI_BUS2}	{GND, GND}: No JTAG {GND, DVDD28}: JTAG at keypad pins {DVDD28, GND}: JTAG at GPIO pins {DVDD28, DVDD28}: JTAG at camera pins

2.4 Analog Baseband

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are some dedicated interfaces for data transfer. The common control interface translates the APB bus write and read cycle for specific addresses related to analog front-end control. During the writing or reading of any of these control registers, there is a latency associated with the transfer of data to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. An analog block includes the following analog functions for the complete GSM/GPRS (2G) baseband signal processing:

1 RF control: DAC for automatic power control (APC) is included, and its output is provided to external RF power amplifier respectively.

2 Auxiliary ADC: Provides an ADC for the battery and other auxiliary analog functions monitoring

3 Audio mixed-signal block: Provides complete analog voice signal processing including microphone amplification, A/D conversion, D/A conversion, earphone driver, etc. Dedicated stereo D/A conversion and amplification for audio signals are also included.

4 Clock generation: Includes a clock squarer for shaping the system clock, and PLL providing clock signals to DSP, MCU and USB unit

5 XOSC32: A 32-kHz crystal oscillator circuit for RTC applications on analog blocks

2.4.1 Auxiliary ADC

1. Block Description

The auxiliary ADC includes the following functional blocks:

6 Analog multiplexer: Selects signal from one of the seven auxiliary input pins. Real-world messages to be monitored, e.g. temperature, should be transferred to the voltage domain.

7 10-bit A/D converter: Converts the multiplexed input signal to 10-bit digital data.

Table 17. Auxillary ADC functional blocks

Channel	Application	Input range [V]
0	BATSNS	3.2 ~ 4.2
1	ISENSE	3.2 ~ 4.2
2	VCDT	Decided by application circuit
3	BATON	0 ~ AVDD28
4	AUXIN4	0 ~ AVDD28
others	Internal use	N/A

2.4.2 32-kHz Crystal Oscillator

2. Block Description

The low-power 32-kHz crystal oscillator XOSC32 is designed to work with an external piezoelectric 32.768 kHz crystal and a load composed of two functional capacitors. See the figure below.

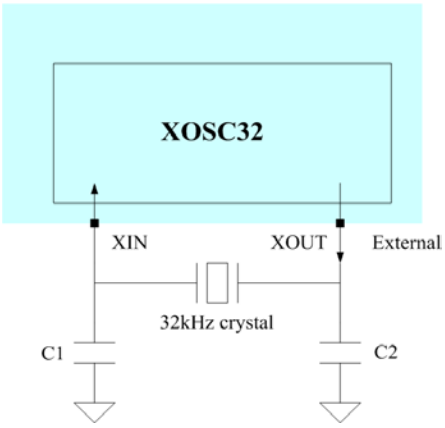


Figure 5. Block diagram of XOSC32

3. Functional Specifications

See the table below for the functional specifications of XOSC32.

Table 18. Functional specifications of XOSC32

Symbol	Parameter	Min.	Typ.	Max.	Unit
AVDDRTC	Analog power supply	1	2.8		V
Tosc	Start-up time			1	sec
Dcyc	Duty cycle	30	50	70	%
	Current consumption			5	μA
T	Operating temperature	-25		70	°C

See the table below for recommendations on crystal parameters to use with XOSC32.

Table 19. Recommended parameters of 32kHz crystal

Symbol	Parameter	Min.	Typ.	Max.	Unit
F	Frequency range		32,768		Hz
GL	Drive level			1	uW
Δf/f	Frequency tolerance		± 20		ppm

Symbol	Parameter	Min.	Typ.	Max.	Unit
ESR	Series resistance		50	70	KΩ
C0	Static capacitance		0.9		pF
CL	Load capacitance		12.5		pF

2.5 Power Management Unit Blocks

The power management unit (PMU) manages the power supply of the entire chip, such as baseband, processor, memory, SIM cards, camera, vibrator, etc. The digital part of PMU is integrated into the analog part. PMU includes the following analog functions for signal processing:

- LDO: Regulates battery voltage to lower voltage level
- Keypad LED driver (KPLED) and current sink (ISINK) switches: Sink current for keypad LED and LCM module
- Start-up (STRUP): Generates power-on/off control sequence of start-up circuits
- Pulse charger (PCHR): Controls battery charging

1.1.1 STRUP

PMU handles the power-on and off of the handset. If the battery voltage is neither in the UVLO state (VBAT ≥ 3.4V) nor in the thermal condition, there are three methods to power on the handset system: pulling PWRKEY low (the user pushes PWRKEY), pulling PWRBB high (baseband BB_WakeUp) or valid charger plug-in.

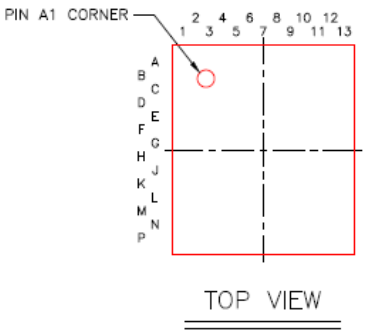
According to different battery voltage (VBAT) and SOC states, control signals and regulators will have different responses.

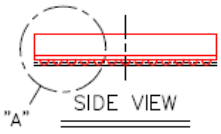
1.1.2 PCHR

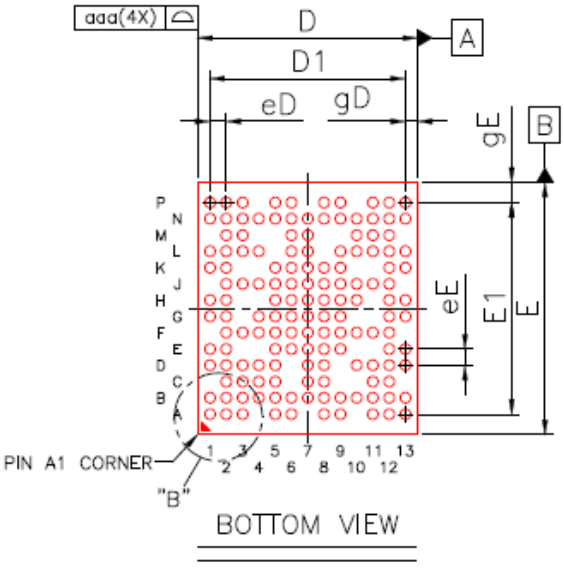
The charger controller senses the charger input voltage from either a standard AC-DC adaptor or an USB charger. When the charger input voltage is within a pre-determined range, the charging process will be activated. This detector can resist higher input voltage than other parts of the PMU.

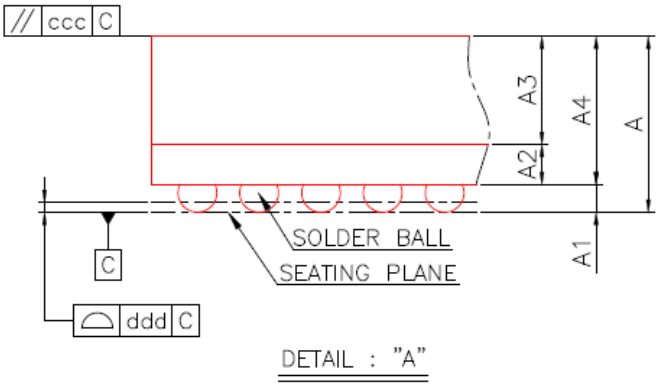
2.6 Package Information

2.6.1 Package Outlines

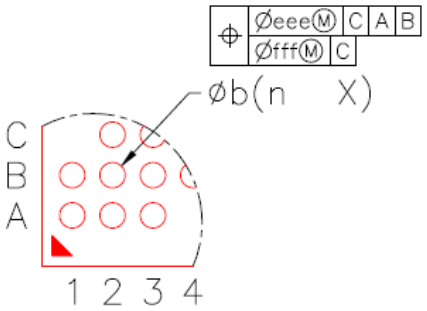








DETAIL : "A"



DETAIL : "B"

Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package Type			VFBGA		
Body Size	X	D	5.30	5.40	5.50
	Y	E	6.10	6.20	6.30
Ball Pitch	X	eD	0.40		
	Y	eE	0.40		
Mold Thickness		A3	0.65 Ref.		
Substrate Thickness		A2	0.11 Ref.		
Substrate+Mold Thickness		A4	0.71	0.76	0.81
Total Thickness		A	–	–	1.00
Ball Diameter			0.25		
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa	0.05		
Mold Flatness		ccc	0.10		
Coplanarity		ddd	0.08		
Ball Offset (Package)		eee	0.15		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	143		
Edge Ball Center to Center	X	D1	4.80		
	Y	E1	5.20		
Edge Ball Center to Package Edge	X	gD	0.30		
	Y	gE	0.50		

Figure 6. Outlines and dimension of TFBGA 5.4mm*6.2mm, 143-ball, 0.4 mm pitch package

2.6.2 Thermal Operating Specifications

Table 20. Thermal Operating Specifications

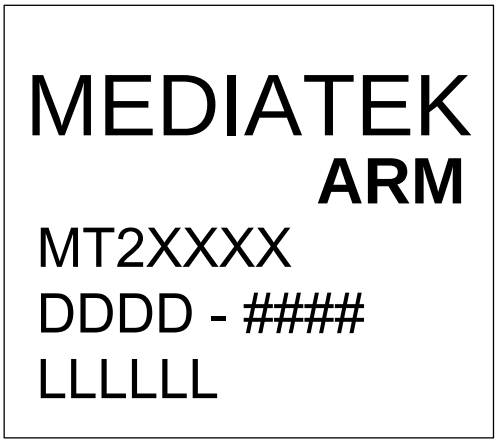
Symbol	Description	Value	Unit	Notes
	Thermal resistance from device junction to package case		C/W	
	Maximum package temperature	65	Deg C	
	Maximum power dissipation	0.33	W	

2.6.3 Lead-free Packaging

MT2502A is provided in a lead-free package and meets RoHS requirements

2.7 Ordering Information

2.7.1 Top Marking Definition



MTXXXXXX Product No.
DDDD: Date Code
####: Subcontractor Code
LLLLLL: Die Lot No.

Figure 7. Mass production top marking of MT2502A

Part number	Package	Description
MT2502A/A	TFBGA	5.4mm*6.2mm, 143-ball, 0.4 mm pitch package, non-security version