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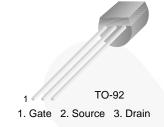


November 2014

BF256B N-Channel RF Amplifiers

Features

- This device is designed for VHF / UHF amplifiers
- Sourced from process 50



Ordering Information

Part Number	Top Mark	Package	Packing Method				
BF256B	BF256B	TO-92 3L	Bulk				

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^{\circ}\text{C}$ unless otherwise noted.

Symbol	Parameter	Value	Unit
V_{DG}	Drain-Gate Voltage	30	V
V_{GS}	Gate-Source Voltage	-30	V
I _{GF}	Forward Gate Current	10	mA
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C

Thermal Characteristics

Values are at $T_A = 25$ °C unless otherwise noted.

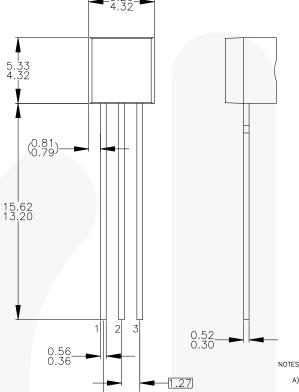
Symbol	Parameter	Value	Unit
В	Total Device Dissipation at T _A = 25°C	350	mW
P_{D}	Derate Above 25°C	2.8	mW/°C

Electrical Characteristics

Values are at $T_A = 25$ °C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Max.	Unit	
V _{(BR)GSS}	Gate-Source Breakdown Voltage	$V_{DS} = 0$, $I_{G} = 1 \mu A$	-30		V	
V_{GS}	Gate-Source Voltage	$V_{DS} = 15 \text{ V}, I_{D} = 200 \mu A$	-0.5	-7.5	V	
V _{GS} (off)	Gate-Source Cut-Off Voltage	V _{DS} = 15 V, I _D = 10 nA	-0.5	-8.0	V	
I _{GSS}	Gate Reverse Current	$V_{GS} = -20 \text{ V}, V_{DS} = 0$		-5	nA	
I _{DSS}	Zero-Gate Voltage Drain Current	V _{DS} = 15 V, V _{GS} = 0	6	13	mA	
gfs	Common Source Forward Transconductance	$V_{DS} = 15 \text{ V}, V_{GS} = 0,$ f= 1 kHz	4.5		mmhos	

Physical Dimensions



2.54

2 3

_4.19 3.05

NOTES: UNLESS OTHERWISE SPECIFIED

- DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
 ALL DIMENSIONS ARE IN MILLIMETERS.
 DRAWING CONFORMS TO ASME Y14.5M-1994.
 TO-92 (92,94,96,97,98) PIN CONFIGURATION:

	ĕ.		92			94			96			97			98	
	₫	Ρ	F	М	Ρ	F	М	В	F	М	Ρ	F	М	Ρ	F	М
	1	Ε	S	S	Ε	S	S	В	D	G	С	G	D	С	G	D
	2	В	D	G	С	G	D	Ε	S	S	В	D	G	Ε	S	S
	3	O	G	D	Φ	D	G	O	G	D	Е	S	S	Ф	D	G
66 13	LE	GEI		POL	AR		E -		MITT	ER		[) -		RAIN	

M - DMOS C - COLLECTOR G - GATE

E) FOR PACKAGE 92, 94, 96, 97 AND 98:
PIN CONFIGURATION DRAIN "D" AND SOURCE "S"
ARE INTERCHANGEAGLE AT JFET "F" OPTION.
F) DRAWING FILENAME: MKT-ZAO3DREV3.

Figure 1. 3-Lead, TO-92, JEDEC TO-92 Compliant Straight Lead Configuration





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