

CMOS Digital Integrated Circuits Silicon Monolithic

TC7WH00FK

1. Functional Description

· Dual 2-Input NAND Gate

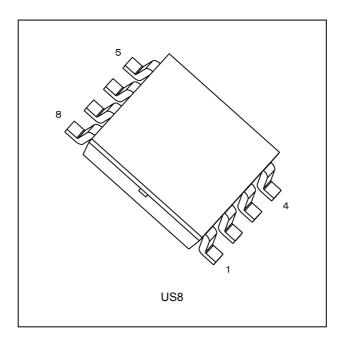
2. Features

- (1) AEC-Q100 (Rev. H) (Note 1)
- (2) Wide operating temperature range: $T_{opr} = -40$ to 125 °C (Note 2)
- (3) High speed operation: $t_{pd} = 3.7 \text{ ns (typ.)}$ ($V_{CC} = 5.0 \text{ V}$, $C_L = 15 \text{ pF}$)
- (4) Low power dissipation: $I_{CC} = 2.0 \mu A \text{ (max) (} T_a = 25 \text{ °C)}$
- (5) High noise immunity: $V_{NIH} = V_{NIL} = 28 \% V_{CC}$ (min)
- (6) 5.5 V tolerant inputs
- (7) Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- (8) Wide operating voltage range: $V_{CC} = 2.0$ to 5.5 V
- (9) Identical pin assignment and function with TC7W00

Note 1: This device is compliant with the reliability requirements of AEC-Q100. For details, contact your Toshiba sales representative.

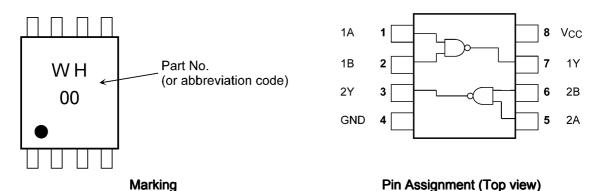
Note 2: For devices with the ordering part number ending in J(CT. T_{opr} = -40 to 85 °C for the other devices.

3. Packaging





4. Marking and Pin Assignment



5. IEC Logic Symbol



6. Truth Table

А	В	Y
L	L	Н
L	Н	Н
Н	L	Н
Н	Н	L

7. Absolute Maximum Ratings (Note) (Unless otherwise specified, Ta = 25 °C)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V _{CC}		-0.5 to 7.0	V
Input voltage	V_{IN}		-0.5 to 7.0	
DC output voltage	V _{OUT}		-0.5 to V _{CC} + 0.5	
Input diode current	I _{IK}		-20	mA
Output diode current	l _{ok}	(Note 1)	±20	
DC output current	l _{out}		±25	
V _{CC} /ground current	I _{CC}		±50	
Power dissipation	P _D		200	mW
Storage temperature	T _{stg}		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: V_{OUT} < GND, V_{OUT} > V_{CC}



8. Operating Ranges (Note)

Characteristics	Symbol	Note	Test Condition	Rating	Unit
Supply voltage	V _{CC}		_	2.0 to 5.5	V
Input voltage	V _{IN}		_	0 to 5.5	
Output voltage	V _{OUT}		_	0 to V _{CC}]
Operating temperature	T _{opr}	(Note 1)	_	-40 to 125	°C
		(Note 2)	_	-40 to 85	
Input rise and fall time	dt/dv		$V_{CC} = 3.3 \pm 0.3 \text{ V}$	0 to 100	ns/V
			$V_{CC} = 5.0 \pm 0.5 \text{ V}$	0 to 20	

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Unused inputs must be tied to either V_{CC} or GND.

Note 1: For devices with the ordering part number ending in J(CT.

Note 2: For devices except those with the ordering part number ending in J(CT.

9. Electrical Characteristics

9.1. DC Characteristics (Unless otherwise specified, $T_a = 25$ °C)

Characteristics	Symbol	Test Condition		V _{CC} (V)	Min	Тур.	Max	Unit
High-level input voltage	V _{IH}	_		2.0	1.5	_	_	V
				3.0 to 5.5	$V_{CC} \times 0.7$	_	_	
Low-level input voltage	V _{IL}	_		2.0	_		0.5	V
				3.0 to 5.5	_	_	$V_{CC} \times 0.3$	
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 μA	2.0	1.9	2.0	_	V
				3.0	2.9	3.0	_	
				4.5	4.4	4.5	_	
			I _{OH} = -4 mA	3.0	2.58	_	_	
			I _{OH} = -8 mA	4.5	3.94	_	_	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH}	I _{OL} = 50 μA	2.0	_	0.0	0.1	V
				3.0	_	0.0	0.1	
				4.5	_	0.0	0.1	
			I _{OL} = 4 mA	3.0	_	_	0.36	
			I _{OL} = 8 mA	4.5	_	_	0.36	
Input leakage current	I _{IN}	V _{IN} = 5.5 V or GND		0 to 5.5			±0.1	μΑ
Quiescent supply current	I _{CC}	$V_{IN} = V_{CC}$ or GND		5.5	_	_	2.0	μΑ



9.2. DC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Cond	dition	V _{CC} (V)	Min	Max	Unit
High-level input voltage	V _{IH}	_		2.0	1.5	_	V
				3.0 to 5.5	$V_{CC} \times 0.7$	_	
Low-level input voltage	V _{IL}	_		2.0	_	0.5	V
				3.0 to 5.5	_	$V_{CC} \times 0.3$	
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 μA	2.0	1.9	_	V
				3.0	2.9	_	
				4.5	4.4	_	
			I _{OH} = -4 mA	3.0	2.48	_	
			$I_{OH} = -8 \text{ mA}$	4.5	3.80	_	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH}	I _{OL} = 50 μA	2.0	_	0.1	V
				3.0	_	0.1	
				4.5	_	0.1	
			I _{OL} = 4 mA	3.0	_	0.44	
			I _{OL} = 8 mA	4.5	_	0.44	
Input leakage current	I _{IN}	V _{IN} = 5.5 V or GND	•	0 to 5.5	_	±1.0	μΑ
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	_	20.0	μΑ

9.3. DC Characteristics (Note) (Unless otherwise specified, T_a = -40 to 125 °C)

Characteristics	Symbol	Test Cond	dition	V _{CC} (V)	Min	Max	Unit
High-level input voltage	V _{IH}	_		2.0	1.5	_	V
				3.0 to 5.5	$V_{CC} \times 0.7$	_	
Low-level input voltage	V _{IL}	_		2.0		0.5	V
				3.0 to 5.5	_	$V_{CC} \times 0.3$	
High-level output voltage	V _{OH}	$V_{IN} = V_{IH}$ or V_{IL}	I _{OH} = -50 μA	2.0	1.9	_	V
				3.0	2.9	_	
				4.5	4.4	_	
			$I_{OH} = -4 \text{ mA}$	3.0	2.40	_	
			I_{OH} = -8 mA	4.5	3.70	_	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH}	I _{OL} = 50 μA	2.0	_	0.1	V
				3.0	_	0.1	
				4.5	_	0.1	
			I_{OL} = 4 mA	3.0	_	0.55	
			$I_{OL} = 8 \text{ mA}$	4.5	_	0.55	
Input leakage current	I _{IN}	V _{IN} = 5.5 V or GND		0 to 5.5	_	±2.0	μΑ
Quiescent supply current	Icc	V _{IN} = V _{CC} or GND		5.5	_	40.0	μΑ

Note: For devices with the ordering part number ending in J(CT.



9.4. AC Characteristics (Unless otherwise specified, $T_a = 25$ °C, Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Note	Test Condition	V _{CC} (V)	C _L (pF)	Min	Тур.	Max	Unit
Propagation delay time	t _{PLH} ,t _{PHL}		_	3.3 ± 0.3	15	_	5.5	7.9	ns
					50	_	8.0	11.4	
				5.0 ± 0.5	15	_	3.7	5.5	
					50	_	5.2	7.5	
Input capacitance	C _{IN}		_			_	4	10	pF
Power dissipation capacitance	C _{PD}	(Note 1)	_			ı	19	ı	pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per 1 gate)}$

9.5. AC Characteristics (Unless otherwise specified, $T_a = -40$ to 85 °C, Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	V _{CC} (V)	C _L (pF)	Min	Max	Unit
Propagation delay time	t _{PLH} ,t _{PHL}	_	3.3 ± 0.3	15	1.0	9.5	ns
				50	1.0	13.0	
			5.0 ± 0.5	15	1.0	6.5	
				50	1.0	8.5	
Input capacitance	C _{IN}	_			_	10	pF

9.6. AC Characteristics (Note) (Unless otherwise specified, T_a = -40 to 125 °C, Input: t_r = t_f = 3 ns)

Characteristics	Symbol	Test Condition	V _{CC} (V)	C _L (pF)	Min	Max	Unit
Propagation delay time	t _{PLH} ,t _{PHL}	_	3.3 ± 0.3	15	1.0	11.0	ns
				50	1.0	14.5	
			5.0 ± 0.5	15	1.0	7.5	
				50	1.0	9.5	
Input capacitance	C _{IN}	_			-	10	pF

Note: For devices with the ordering part number ending in J(CT.

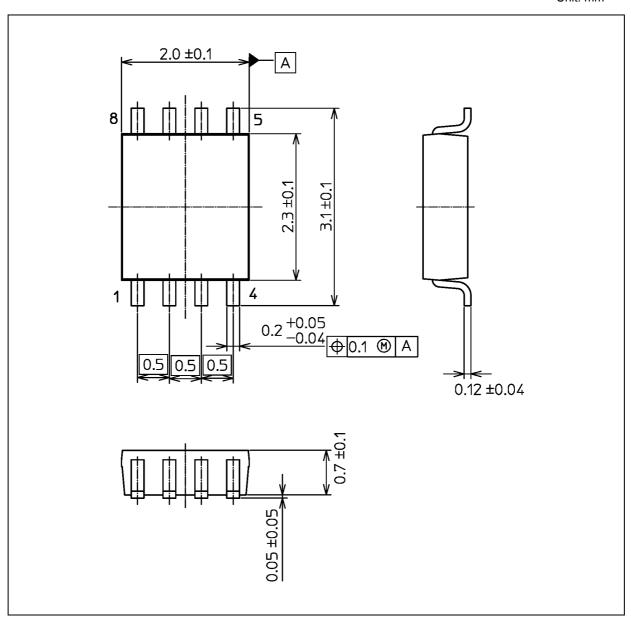
9.7. Noise Characteristics (Unless otherwise specified, $T_a = 25$ °C, Input: $t_f = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Тур.	Limit	Unit
Quiet output maximum dynamic V _{OL}	V _{OLP}	C _L = 50 pF	5.0	0.3	0.8	V
Quiet output minimum dynamic V _{OL}	V _{OLV}	C _L = 50 pF	5.0	-0.3	-0.8	V
Minimum high-level dynamic input voltage	V_{IHD}	C _L = 50 pF	5.0	_	3.5	V
Maximum low-level dynamic input voltage	V_{ILD}	C _L = 50 pF	5.0		1.5	V



Package Dimensions

Unit: mm



Weight: 0.01 g (typ.)

Package Name(s)
JEDEC: SOT-765
Nickname: US8



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