

AD9741/3/5/6/7 Evaluation Board Quick Start Guide

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Getting Started with the AD9741/3/5/6/7 Evaluation Board

WHAT'S IN THE BOX AD9747-EBZ Evaluation Board Mini-USB Cable AD9747 Evaluation Board CD

EXAMPLE EQUIPMENT LIST

+5Vdc Power Supply: Agilent E3630A Digital Pattern Generator (DPG2): ADI HSC-DAC-DPG-BZ DAC Clock Source: R&S SML 02 AQM LO Clock Source: R&S SMA100A Spectrum Analyzer: Agilent PSAA or R&S FSU PC: Windows PC with 2 or more USB ports (See Appendix for system requirements)

INTRODUCTION

The AD9747 Evaluation Board connects to the Analog Devices Digital Pattern Generator (DPG2) to allow for quick evaluation of the AD9747. The DPG2 allows the user to create many types of digital vectors and transmit these at speed to the AD9747 in any of the AD9747 operating modes. The AD9747 evaluation board is configured over USB from a panel within the DPGDownloader software.

(Note: The AD9747 operation is described in detail. The operation of the other devices in the family is described in a later section.)

SOFTWARE INSTALLATION

The AD9747 application software, DPGDownloader, should be installed on the PC prior connecting the hardware to the PC. The DAC Software Suite is included on the Evaluation Board CD, or can be downloaded from the DPG web site at http://www.analog.com/dpg. This will install DPGDownloader required for loading vectors into the DPG2 and configuring the AD9747 evaluation board.

HARDWARE SETUP (DAC OUTPUT)

Once the DPGDownloader software is installed, the hardware can be connected as shown in Figure 1. A single 5V power supply powers the evaluation board. The power supply should be able to source up to 1A to cover all of the board's operating conditions. A low jitter clock source (< 0.5psec RMS) should be used for the DACCLK. A sinusoidal clock output level of 0 to 4dBm is optimal. By default, the DAC outputs are connected to SMA connectors for evaluation. Both DAC outputs are available. Later in document, the modifications for observing the modulator output and different clocking options will be shown. The evaluation board plugs directly into the DPG2. The PC connects to both the DPG2 and the evaluation board through USB cables.



Figure 1- Bench Set-Up



Figure 2- DPG2 and AD9747 Evaluation Board

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GETTING STARTED – SINGLE TONE TEST

It is suggested that the basic set-up is verified before making any modifications to the evaluation board.

Basic Hardware Set-Up

Connect the equipment to the AD9747 evaluation board per the following table:

Equipment	Connects to AD9747 Eval Board
Power Supply)	P5 (+5V), P6 (GND
Signal Source	J1 (CLOCK IN), Set source to 100MHz, 2dBm output
PC USB Cable	XP2
Spectrum Analyzer	J5 (IOUT1_P) or J9 (IOUT2_P)
DPG2	P1 and P2

DPGDownloader Software

Power up the DPG and connect the USB cable to the PC. Next, run the DPGDownloader Software. A shortcut will be installed to your Start menu during the installation of the DAC Software Suite. To begin, click on the DPGDownloader shortcut in your Programs menu, typically at Start > Programs > Analog Devices > DPG > DPGDownloader.

The basic parts of the DPGDownloader window are; Hardware Config Panel, EVB Config, Vector Generation Pull-Down Menu, Vector Palette, Vector Selection Panel and the Download and Play buttons.



Figure 3 – DPGDownloader Window

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Quick Start Guide

- If the AD9747 evaluation board has been recognized by the PC, "AD9747 RevB" should be populated in the Evaluation Board field in the Hardware Config panel.
- Generate a sinewave by pulling down the "Add Generated Waveform" menu and choosing "Single Tone". Fill in the form as shown in Figure 3 (Sample Rate = 100MHz, Desired Frequency = 17.0MHz, etc.). Select the I and Q data vectors in the data selection panel.
- Configure the eval board by writing the value 01 to register 1E1. This configures the AD9516 to use the CLK input to drive the clock path.

SPI Control	Data Control	Fower Down	DAC Mode	DAC Gain	Aux DACs	AD9516-General	AD9516-DAC Clock	AD9516-Modulator LO	Clock
-PLL & VCO VCD Divide	er: +4	Addrese:	Access 1E1 00 00 00 00					Soft Reset	Commit Write
			YVIII	<u> </u>					Auto-Com

Bypass the clock dividers on the AD9516.

SPI Control	Data Control	Power Down	DAC Mode	DAC Gain	Aux DACs /	AD9516-0	ieneral	AD9516-DAC Clock AD9516-Modulator LO Clock
Divider 1:	Low Cycles:	2	High Cyclee:	2	Phase Offset:	0	*	Вуразе
Divider 2:	Low Cycles:	1 🗘	High Cycles:	1 🗘	Phase Offset:	0	•	Bypass
Power-D	own Clock Out	out						

- The DCO frequency field in the DPGDownloader window should now be reading something close to 100MHz.
- Next hit the download 💷 button. This transfers the data from the PC to the DPG memory.
- When the vector has finished downloading, hit the play button. This starts the DPG2 transmitting data to the eval board.
- The output from J5 and J9 should be a clean 29MHz tone as shown below:



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Using the AD9741/AD97473/AD9745/AD9746 Evaluation Boards

The evaluation boards for the AD9741/AD97473/AD9745/AD9746/AD9747 are identical except for the DUT installed. The operation of the eval boards is also the same except for the vector generation "DAC Resolution" field and the Data Width fields as shown below. These fields should be configured to match the DUT.

add Data Hile 🔻 🥁 Add Generated Wavef	rm 🔻 ၊ 👗 Remove Selec	ted Remove Al	dis-	_	_					Graph Selec
Sample Rate: 100.000 h Desired Frequency: 17.000 h Calculated Frequency: 16.95	Hz DAC Resoluti Hz Amplitude: B MHz Cycles:	on: 16 🗢 bits 0.0 🗢 dB (Fu 2785	Re Ill Scale) Re Unsigned Da Allow even c	cord Length: lative Phase: ta ycle count	16384 0.0	Complex Da	ta (I&C)		Savet
stion Board: AD9747 RevB 💌 🛠	SPI Control Data C Divider 1: Low C Divider 2: Low C	ontrol Power Dowr ycles: 2 🗢	High Cycles: 2	DAC Gain A 2 💠 PH	Aux DACs	AD9516-Gene	eral A	09516-DAC Clock pass	AD9516-Modulato	r L0 Clock
Cont 1 AD3747 RevB V % onfiguration: Cocced via data corne V uration Progess: 162.1.0 12/2/2008 JPG Sync: Single V	SPI Control Data C Divider 1: Low C Divider 2: Low C Divider 2: Low C Power-Down Oc	ontrol Power Down yoles: 2 2 yoles: 1 2 ck Output	High Cycles: 2 High Cycles: 1	DAC Gain A 2 🗘 Pi I 🗘 Pi	Aux DACs // 'hase Offset:	AD9516-Gene 0 \$ 0 \$	eral (A) 🖓 Þ, 🖓 Þ,	09515-DAC Clock pass pass	AD9516-Modulato	r LO Clock
2 Unit 1 ADS747 RevB ADS747 R	SPI Control Data C Divider 1: Low C Divider 2: Low C Power-Down Clo Data Playback Data Playback	ontrol Power Dowr ysles: 2 ysles: 1 ck Output	DAC Mode High Cycles: 2 High Cycles: 1 8 MHz; 0.0 dB; 0 98 MHz; 0.0 dB; 0	DAC Gain A 2 \$ Pt 1 \$ Pt .0° (In-Phase) 0.0° (Quadratu	Aux DACs // hase Offset: hase Offset:) ura)	AD9516-Gene	eral A	09515-DAC Clock	AD9516-Modulato	r L0 Clock
Cont I Ab3747 RevB ♥ ♥ withon Board: Ab3747 RevB ♥ ♥ withon Program uration Version: Clocked vis data conne ♥ uration Version: 16.2.1.0 12/2/2008 PGS sync: Single ♥	SPI Control Data C Divider 1: Low C Divider 2: Low C Power-Down Oc Data Playback 1 Data Vector: 11: 0 Data Vector: 10 Play Mode: Lo Stat Offset:	ontrol Power Down yoles: 2 yoles: 1 ck Output Single Tone - 15.99 single Tone - 15.99 c Output 0 0 0	DAC Mode 1 High Cycles: 2 High Cycles: 1 8 MHz; 0.0 dB; 0 98 MHz; 0.0 dB; 1 ount:	DAC Gain (A 2	Aux DACs / / hase Offset : hase Offset :) ure)	AD9516-Gen	eral (A)	99515-DAC Clock	AD9516-Modulato	r LO Clock

Selecting the Modulator Outputs

By default, solder jumpers JP4, JP5, JP6, and JP7 configure the DAC outputs to be observed at SMA outputs J5 and J9. This jumper setting is shown in Figure 4 a). To connect the DAC outputs to the LPF and the ADL537x analog quadrature modulator, the solder jumpers need to be repositioned as shown in Figure 4 b). The modulator output can be observed thru the SMA connector J6 (MODULATED OUTPUT). The modulator LO input can be sourced thru SMA connector J10 (LOCAL OSC INPUT). The clock level into the modulator should be set to about 3dBm.





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Eval Board Jumper Options

There are 6 pin jumpers on the evaluation board corresponding to the 6 supplies on the board. They serve as 'switches' that determine if the LDOs on board or external supplies are used for each individual supply. They are shunted by default, which means on board LDOs are used. When an external supply is necessary, pull off the shunt from the corresponding supply and connect the external supply to the SMA test points close to the jumper.

Table 1 – Pin Jumper configuration Options

Supply Rail	For LDO, Install Pin Jumper	For external Supply, use Test Points
CVDD18	JP10	TP1(+1.8V), TP2 (GND)
DVDD18	JP11	TP3(+1.8V), TP4 (GND)
DVDD33	JP12	TP5(+3.3V), TP6 (GND)
AVDD33	JP13	TP7(+3.3V), TP8 (GND)
CVDD33	JP14	TP9 (+3.3V), TP10 (GND)
AVDD5	JP15	TP11(+5V), TP12 (GND)



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Appendix A – DPGDownloader Notes

Detailed documentation for the DPGDownloader Software and the Full DPG Suite can be accessed thru the Help Pull-down menu. Also available from the Help pull-down menu is the "Check for Updates" shortcut for checking to see if there is a more recent DPGDownloader version available with an option to automatically update the software.



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