



ALPHA & OMEGA
SEMICONDUCTOR

AOC3860A

12V Common-Drain Dual N-Channel MOSFET

General Description

- Trench Power MOSFET technology
- Low $R_{SS(ON)}$
- With ESD protection to improve battery performance and safety
- Common drain configuration for design simplicity
- RoHS and Halogen-Free Compliant

Applications

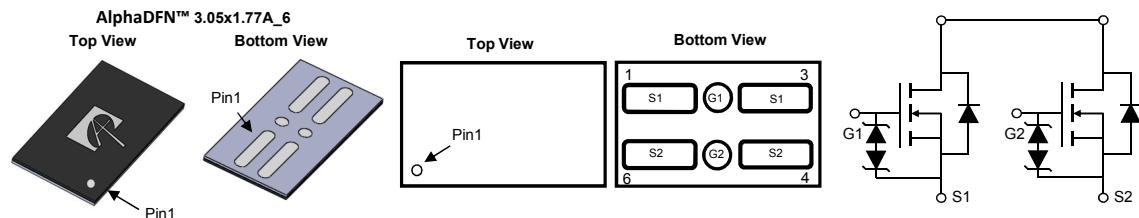
- Battery protection switch
- Mobile device battery charging and discharging

Product Summary

V_{SS}	12V
$R_{SS(ON)}$ (at $V_{GS}=4.5V$)	< 3.5mΩ
$R_{SS(ON)}$ (at $V_{GS}=4.0V$)	< 3.7mΩ
$R_{SS(ON)}$ (at $V_{GS}=3.8V$)	< 3.75mΩ
$R_{SS(ON)}$ (at $V_{GS}=3.1V$)	< 4.3mΩ
$R_{SS(ON)}$ (at $V_{GS}=2.5V$)	< 5mΩ

Typical ESD protection

HBM Class 2



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOC3860A	AlphaDFN 3.05x1.77A_6	Tape & Reel	8000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Rating	Units
Source-Source Voltage	V_{SS}	12	V
Gate-Source Voltage	V_{GS}	± 8	V
Source Current(DC) ^{Note1}	I_S $T_A=25^\circ\text{C}$	25	A
Source Current(Pulse) ^{Note2}	I_{SM}	100	
Power Dissipation ^{Note1}	P_D $T_A=25^\circ\text{C}$	2.5	W
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Typical	Units
Maximum Junction-to-Ambient	$t \leq 10\text{s}$	$R_{\theta JA}$	$^\circ\text{C/W}$
Maximum Junction-to-Ambient	Steady-State	50	$^\circ\text{C/W}$

Note 1. I_S rated value is based on bare silicon. Mounted on 70mmx70mm FR-4 board.

Note 2. PW <10 μs pulses, duty cycle 1% max.

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
STATIC PARAMETERS							
BV_{SSS}	Source-Source Breakdown Voltage	$I_S=250\mu\text{A}, V_{GS}=0\text{V}$	Test Circuit 6	12		V	
I_{SSS}	Zero Gate Voltage Source Current	$V_{SS}=12\text{V}, V_{GS}=0\text{V}$	Test Circuit 1		1	μA	
			$T_J=55^\circ\text{C}$		5		
I_{GSS}	Gate leakage current	$V_{SS}=0\text{V}, V_{GS}=\pm 8\text{V}$	Test Circuit 2		± 10	μA	
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{SS}=V_{GS}, I_S=250\mu\text{A}$	Test Circuit 3	0.3	0.6	1.0	V
$R_{SS(\text{ON})}$	Static Source to Source On-Resistance	$V_{GS}=4.5\text{V}, I_S=5\text{A}$	Test Circuit 4	2.0	2.8	3.5	$\text{m}\Omega$
		$T_J=125^\circ\text{C}$		2.7	3.85	4.8	
		$V_{GS}=4.0\text{V}, I_S=5\text{A}$	Test Circuit 4	2.1	2.9	3.7	$\text{m}\Omega$
		$V_{GS}=3.8\text{V}, I_S=5\text{A}$	Test Circuit 4	2.2	2.95	3.75	$\text{m}\Omega$
		$V_{GS}=3.1\text{V}, I_S=5\text{A}$	Test Circuit 4	2.3	3.2	4.3	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{SS}=5\text{V}, I_S=5\text{A}$	Test Circuit 4	2.5	3.6	5.0	$\text{m}\Omega$
			Test Circuit 3		70		
V_{FSS}	Forward Source to Source Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$	Test Circuit 5		0.56	1	V
DYNAMIC PARAMETERS							
R_g	Gate resistance	$f=1\text{MHz}$			1.2	$\text{k}\Omega$	
SWITCHING PARAMETERS							
Q_g	Total Gate Charge	$V_{G1S1}=4.5\text{V}, V_{SS}=6\text{V}, I_S=5\text{A}$		44		nC	
$t_{D(\text{on})}$	Turn-On DelayTime	$V_{G1S1}=4.5\text{V}, V_{SS}=6\text{V}, R_L=1.2\Omega,$ $R_{\text{GEN}}=3\Omega$	Test Circuit 8	2		μs	
t_r	Turn-On Rise Time			4.5		μs	
$t_{D(\text{off})}$	Turn-Off DelayTime			6		μs	
t_f	Turn-Off Fall Time			11		μs	

APPLICATIONS OR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

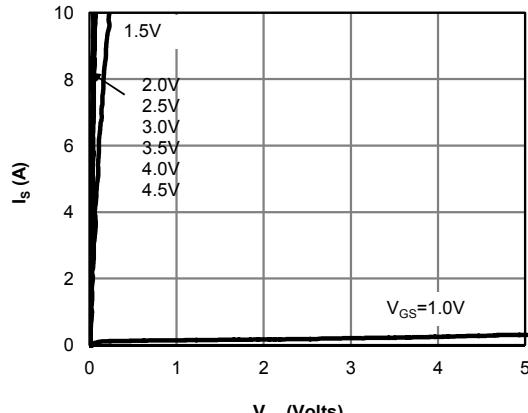


Figure 1: On-Region Characteristics

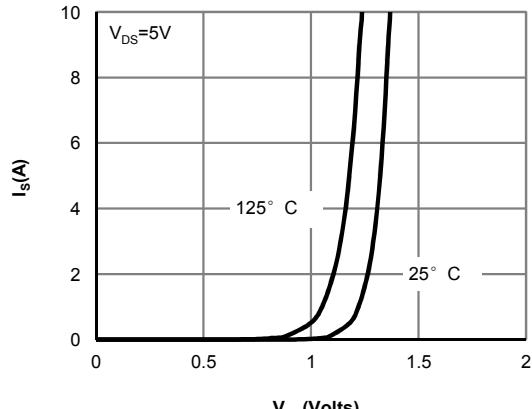


Figure 2: Transfer Characteristics

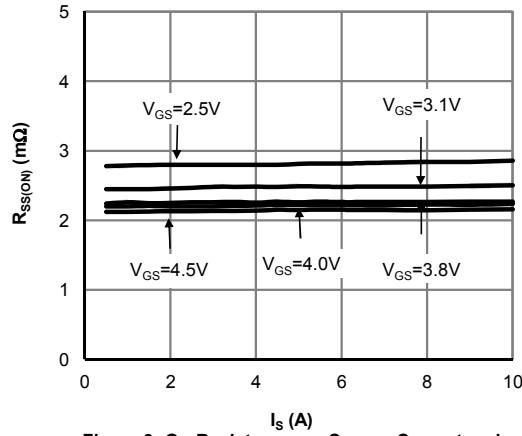


Figure 3: On-Resistance vs. Source Current and Gate Voltage

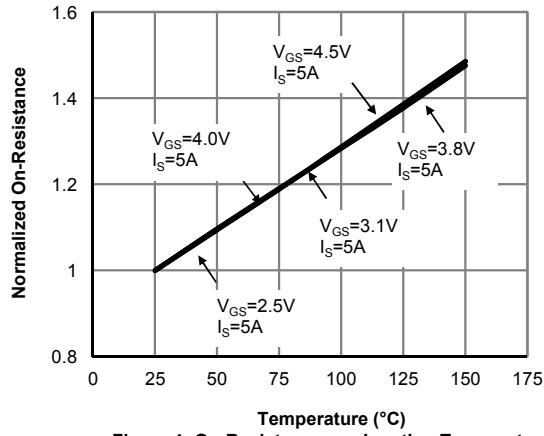


Figure 4: On-Resistance vs. Junction Temperature

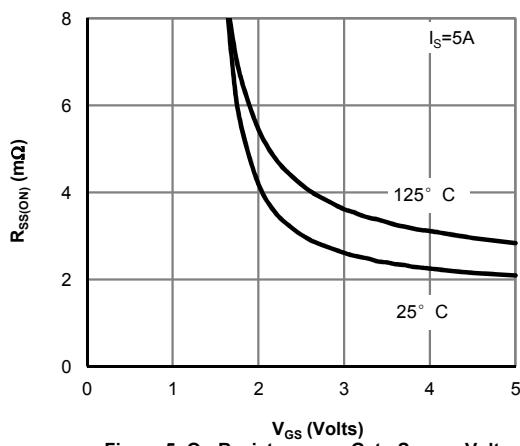


Figure 5: On-Resistance vs. Gate-Source Voltage

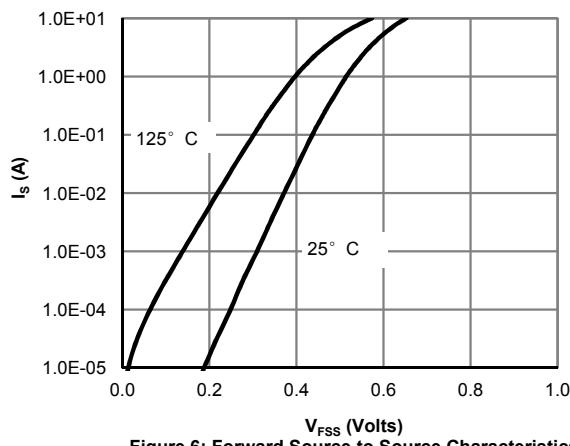


Figure 6: Forward Source to Source Characteristics



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

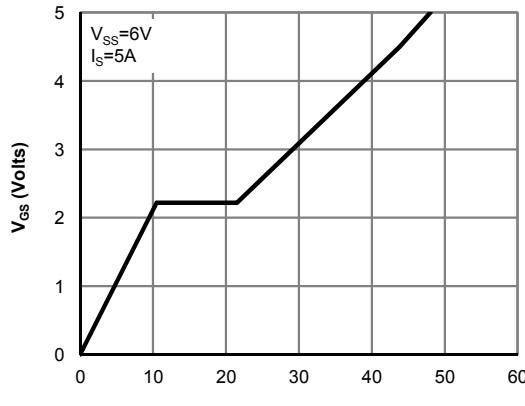


Figure 7: Gate-Charge Characteristics

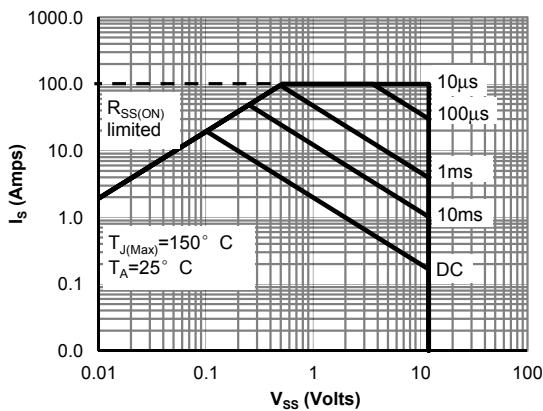


Figure 8: Maximum Forward Biased Safe Operating Area (Note1)

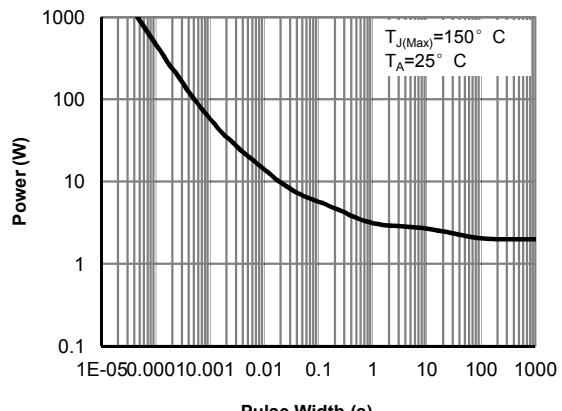


Figure 9: Single Pulse Power Rating Junction-to-Ambient (Note1)

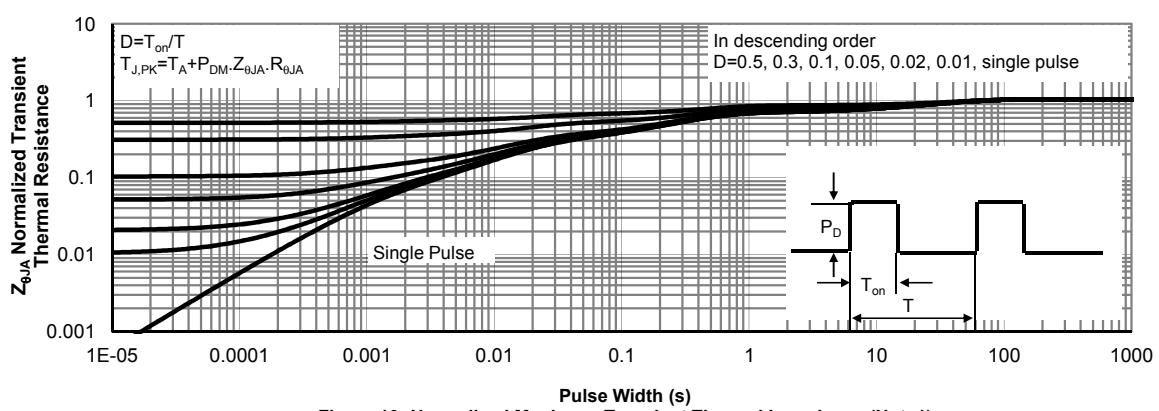
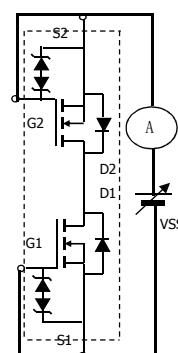


Figure 10: Normalized Maximum Transient Thermal Impedance (Note1)

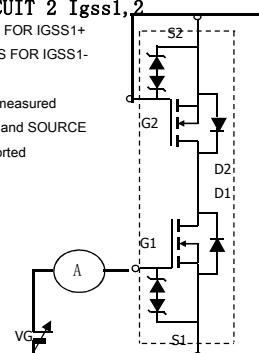


TEST CIRCUIT 1 Isss
POSITIVE VSS FOR ISSS+
NEGATIVE VSS FOR ISSS-



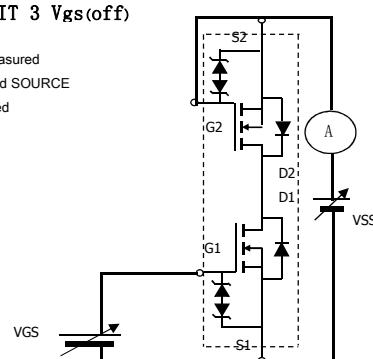
TEST CIRCUIT 2 Igss1,2
POSITIVE VGS FOR IGSS1+
NEGATIVE VGS FOR IGSS1-

When FET1 is measured
between GATE and SOURCE
of FET2 are shorted



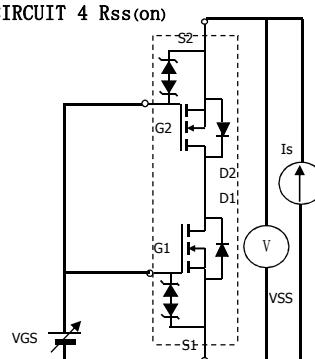
TEST CIRCUIT 3 Vgs(off)

When FET1 is measured
between GATE and SOURCE
of FET2 are shorted



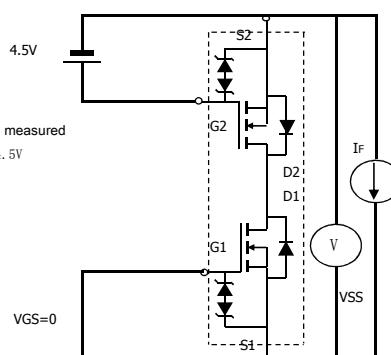
TEST CIRCUIT 4 Rss(on)

Vss/Is



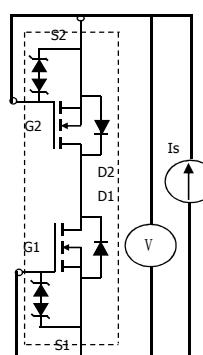
TEST CIRCUIT 5 VF(ss)1,2

When FET1 measured
FET2 VGS=4.5V



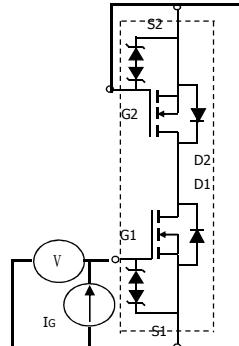
TEST CIRCUIT 6 BVdss

POSITIVE VSS FOR ISSS+
NEGATIVE VSS FOR ISSS-



TEST CIRCUIT 7 BVgs01,2
POSITIVE VSS FOR ISSS+
NEGATIVE VSS FOR ISSS-

When FET1 is measured
between GATE and SOURCE
of FET2 are shorted



TEST CIRCUIT 8
Switching time

