Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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DATA SHEET



MOS FIELD EFFECT TRANSISTOR

NP80N055ELE, NP80N055KLE

NP80N055CLE, NP80N055DLE, NP80N055MLE, NP80N055NLE

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

These products are N-channel MOS Field Effect Transistors designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE	
NP80N055ELE-E1-AY Note1, 2			TO-263 (MP-25ZJ) typ. 1.4 g	
NP80N055ELE-E2-AY Note1, 2	Duro Cn (Tin)	Tape 800 p/reel		
NP80N055KLE-E1-AY Note1	Pure Sn (Tin)		TO-263 (MP-25ZK) typ. 1.5 g	
NP80N055KLE-E2-AY Note1				
NP80N055CLE-S12-AZ Note1, 2	Sn-Ag-Cu		TO-220 (MP-25) typ. 1.9 g	
NP80N055DLE-S12-AY Note1, 2		Tuba 50 a/tuba	TO-262 (MP-25 Fin Cut) typ. 1.8 g	
NP80N055MLE-S18-AY Note1	Pure Sn (Tin)	Tube 50 p/tube		TO-220 (MP-25K) typ. 1.9 g
NP80N055NLE-S18-AY Note1			TO-262 (MP-25SK) typ. 1.8 g	

Notes 1. Pb-free (This product does not contain Pb in the external electrode.)

2. Not for new design

FEATURES

- Channel temperature 175 degree rated
- Super low on-state resistance

 $R_{DS(on)1} = 11 \text{ m}\Omega$ MAX. (Vgs = 10 V, ID = 40 A)

 $R_{DS(on)2}$ = 13 $m\Omega$ MAX. (VGS = 5 V, ID = 40 A)

 $R_{DS(on)3}$ = 15 m Ω MAX. (VGS = 4.5 V, ID = 40 A)

• Low input capacitance

Ciss = 2900 pF TYP.

• Built-in gate protection diode

(TO-220)



(TO-262)



(TO-263)



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ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (V _{GS} = 0 V)	VDSS	55	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C) Note1	I _{D(DC)}	±80	Α
Drain Current (Pulse) Note2	I _{D(pulse)}	±200	Α
Total Power Dissipation (Tc = 25°C)	Рт	120	W
Total Power Dissipation (T _A = 25°C)	Рт	1.8	W
Channel Temperature	Tch	175	°C
Storage Temperature	Tstg	-55 to +175	°C
Single Avalanche Current Note3	las	45/30/10	Α
Single Avalanche Energy Note3	Eas	2.0/90/100	mJ

Notes 1. Calculated constant current according to MAX. allowable channel temperature.

- **2.** PW \leq 10 μ s, Duty cycle \leq 1%
- 3. Starting T_{ch} = 25°C, V_{DD} = 28 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V (see Figure 4.)

THERMAL RESISTANCE

Channel to Case Thermal Resistance	Rth(ch-C)	1.25	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A)	83.3	°C/W

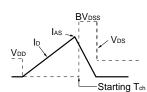


ELECTRICAL CHARACTERISTICS (TA = 25°C)

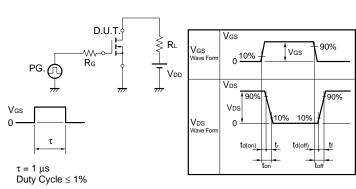
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	Ipss	V _{DS} = 55 V, V _{GS} = 0 V			10	μА
Gate Leakage Current	Igss	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μА
Gate to Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.5	2.0	2.5	V
Forward Transfer Admittance	yfs	V _{DS} = 10 V, I _D = 40 A	15	40		S
Drain to Source On-state Resistance	RDS(on)1	V _{GS} = 10 V, I _D = 40 A		8.4	11	mΩ
	RDS(on)2	V _{GS} = 5 V, I _D = 40 A		10.3	13	mΩ
	RDS(on)3	V _{GS} = 4.5 V, I _D = 40 A		11.3	15	mΩ
Input Capacitance	Ciss	V _{DS} = 25 V,		2900	4400	pF
Output Capacitance	Coss	V _{GS} = 0 V,		380	570	pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		170	310	pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 28 V, I _D = 40 A,		22	48	ns
Rise Time	tr	V _{GS} = 10 V,		10	25	ns
Turn-off Delay Time	t _{d(off)}	R _G = 1 Ω		62	120	ns
Fall Time	tf			11	27	ns
Total Gate Charge	Q _{G1}	V _{DD} = 44 V, V _{GS} = 10 V, I _D = 80 A		50	75	nC
	Q _{G2}	V _{DD} = 44 V,		26	39	nC
Gate to Source Charge	QGS	V _{GS} = 5 V,		12		nC
Gate to Drain Charge	Q _{GD}	I _D = 80 A		15		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 80 A, V _{GS} = 0 V		1.0		V
Reverse Recovery Time	trr	IF = 80 A, VGS = 0 V,		50		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		100		nC

TEST CIRCUIT 1 AVALANCHE CAPABILITY

$V_{GS} = 20 \rightarrow 0 \text{ V}$ $PG. \bigcirc PG. \bigcirc PG.$



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE

$$\begin{array}{c|c} D.U.T. \\ \hline \\ IG = 2 \text{ mA} \\ \hline \\ VOD \end{array}$$

TYPICAL CHARACTERISTICS (TA = 25°C)

Figure 1. DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

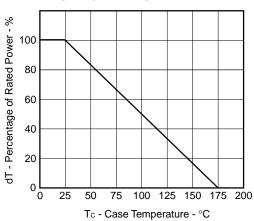
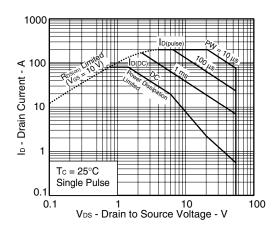


Figure3. FORWARD BIAS SAFE OPERATING AREA



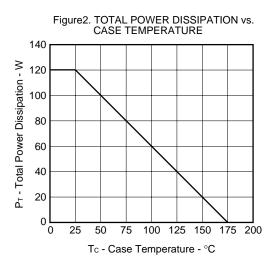


Figure 4. SINGLE AVALANCHE ENERGY DERATING FACTOR

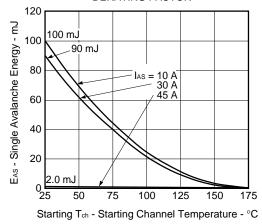


Figure 5. TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

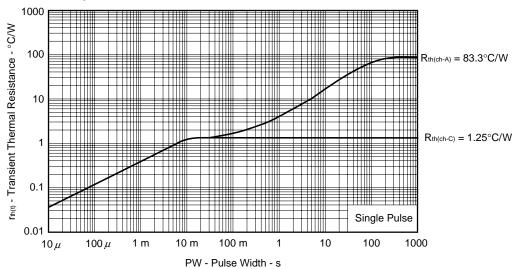


Figure 6. FORWARD TRANSFER CHARACTERISTICS

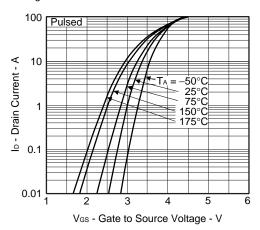


Figure 8. FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

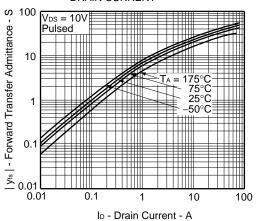


Figure 10. DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

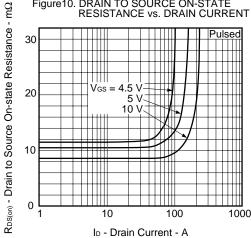


Figure7. DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

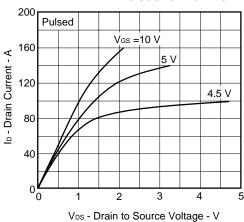


Figure9. DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

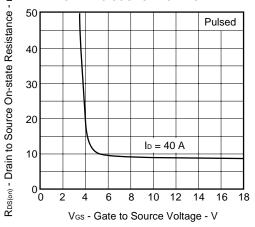
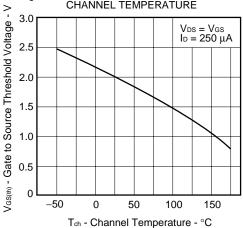


Figure 11. GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



 $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}$ - Drain to Source On-state Resistance - $m\Omega$

Figure 12. DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE

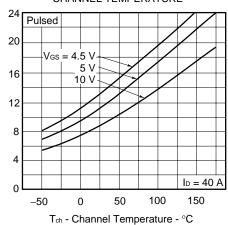


Figure13. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

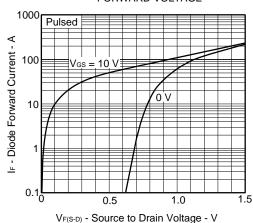


Figure14. CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

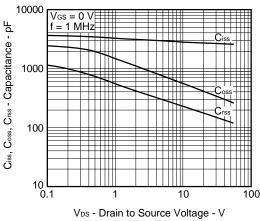


Figure 15. SWITCHING CHARACTERISTICS

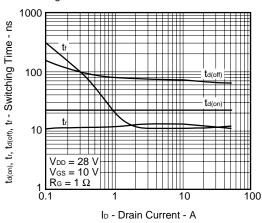


Figure 16. REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

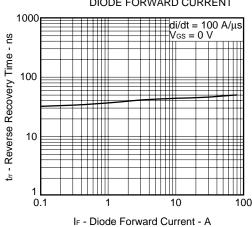
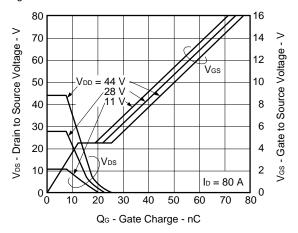
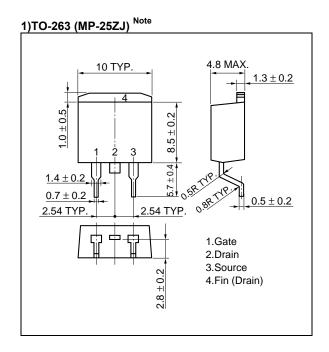
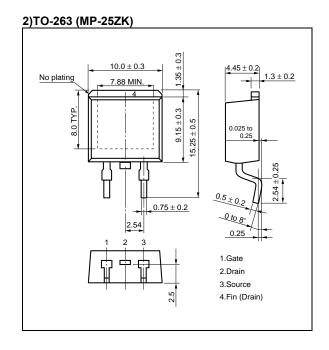


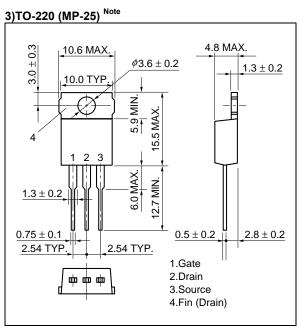
Figure 17. DYNAMIC INPUT/OUTPUT CHARACTERISTICS

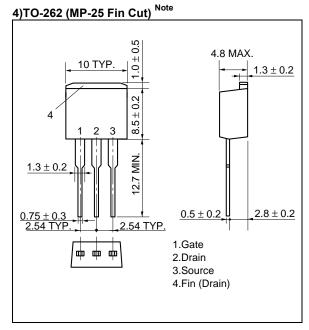


<R> PACKAGE DRAWINGS (Unit: mm)

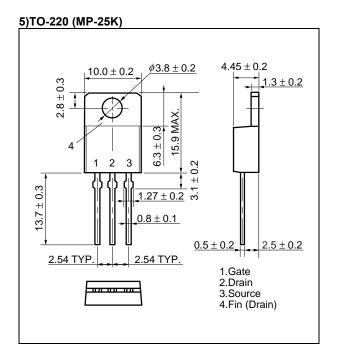


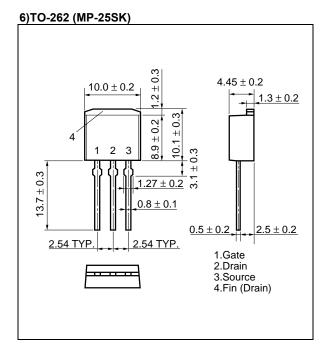




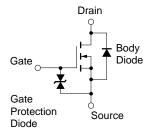


Note Not for new design





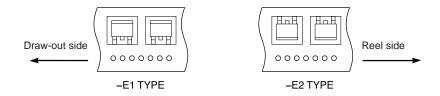
EQUIVALENT CIRCUIT



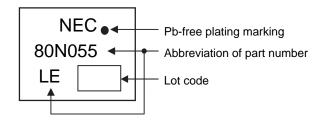
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

<R> TAPE INFORMATION

There are two types (-E1, -E2) of taping depending on the direction of the device.



<R> MARKING INFORMATION



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These products should be soldered and mounted under the following recommended conditions.

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For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Soldering Method	Soldering Conditions	Recommended Condition Symbol	
Infrared reflow	Maximum temperature (Package's surface temperature): 260°C or below		
MP-25ZJ, MP-25ZK	Time at maximum temperature: 10 seconds or less		
	Time of temperature higher than 220°C: 60 seconds or less	IR60-00-3	
	Preheating time at 160 to 180°C: 60 to 120 seconds		
	Maximum number of reflow processes: 3 times		
	Maximum chlorine content of rosin flux (percentage mass): 0.2% or less		
Wave soldering	Maximum temperature (Solder temperature): 260°C or below		
MP-25, MP-25K, MP-25SK,	Time: 10 seconds or less	THDWS	
MP-25 Fin Cut	Maximum chlorine content of rosin flux: 0.2% (wt.) or less		
Partial heating	Maximum temperature (Pin temperature): 350°C or below		
MP-25ZJ, MP-25ZK,	Time (per side of the device): 3 seconds or less	P350	
MP-25K, MP-25SK	Maximum chlorine content of rosin flux: 0.2% (wt.) or less		
Partial heating	Maximum temperature (Pin temperature): 300°C or below		
MP-25, MP-25 Fin Cut	Time (per side of the device): 3 seconds or less	P300	
	Maximum chlorine content of rosin flux: 0.2% (wt.) or less		

Caution Do not use different soldering methods together (except for partial heating).

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