Installation Instructions for the SS421L/SS421H Series



🛦 WARNING

PERSONAL INJURY

DO NOT USE these products as safety or emergency stop devices or in any other application where failure of the product could result in personal injury. **Failure to comply with these instructions**

could result in death or serious injury.

SOLDERING INSTRUCTIONS

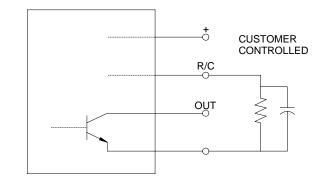
Through-hole leads: Wave solder at 250 °C to 260 °C [482 °F to 500 °F] for a maximum of three seconds.

Surface-mount listings: Use infrared reflow process with peak temperatures not to exceed 245 °C [473 °F].

CLEANING

Use agitated rinse. **Do not use pressure wash.** High-pressure stream could force contaminants into package.

ABSOLUTE MAXIMUM RATINGS^(Note 1)



BLOCK DIAGRAM CURRENT SOURCING OUTPUT



Parameter	Min	Max	Unit	Conditions
Ambient Temperature	-40	+125	°C	Storage, no power applied
Ambient Temperature	-40	+105	°C	Operating, power applied
Supply Voltage	-25	+25	Vdc	-40 °C to +105 °C ambient temperature
Voltage at Output	-0.5	+25	Vdc	Off condition of output over temperature
Open Collector NPN	-	+20	mA	Operated over temperature, current sinking output inverted or non-inverted

Notes:

1. Absolute maximum ratings are the extreme limits the device will withstand without damage to the device. However, the electrical and mechanical characteristics are not guaranteed as the maximum limits (above recommended operating conditions) are approached, nor will the device necessarily operate at absolute maximum ratings.

ELECTRICAL CHARACTERISTICS^(Note 1) (Required -25 °C to +105 °C ambient.)

Parameter	Min	Max	Unit	Conditions	
Supply Voltage (Vs)	4.5	16	Vdc	_	
Supply Current (Is)	_	15	mA	Output released, Vs = 16 V, T ₁ = +25 °C	
		15	mA	,	
Supply Current (Is)	_	15	mA	Output operated, Vs = 16 V, T ₁ = +25 °C	
		15	mA	· ·	
Output Voltage	-	0.4	Vdc	Sinking 15 mA, Vsat	
Output Leakage Current	-	10	μA	Output at 25 V	
Rise Time (10% to 90%)	-	1.5	μs	Vs = 12 V, R = 800 ohms, C = 50 pf	
Fall Time (90% to 10%)	_	1.5	μs	Vs = 12 V, R = 800 ohms, C = 50 pf	

Notes:

1. Over operating temperature and voltage range unless otherwise noted.

SS421L/SS421H Series

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Parameter	Min	Max	Unit	Conditions	
Operate Point	-	250	G	Ta = +25 °C, Note 2	
Operate Point	-	250	G	25 °C to 105 °CV	
Release Point	-250	_	G	Ta = +25 °C	
Release Point	-250			-25 °C to 105 °C, Note 3	
Differential	50	_	G	Operate minus release	

Notes:

1. Over operating temperature and voltage range unless otherwise noted.

2. Operate point is defined as the gauss level above which the internal circuitry will always be indicating the presence of a south pole at the IC surface.

3. Release point is defined as the gauss level below which the internal circuitry will always be indication the presence of a north pole at the IC surface.

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Min	Max	Unit	Conditions
1800	5200	PPM	Ta = +25 °C, Note 2
-16.0	16.0	%	Variation from calculated value, Note 3
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5.0	16.0	sec	Ta = +25 °C, 1800 to 5200 PPM
	1.2	sec	Ta = +25 °C, 1800 to 5200 PPM, Note 4
			% of delay set time
-40	+40	%	
-4.0	4.0	sec	
-	20	%	% of delay set time, Note 5
nt –	0.05	_	Note 6
	Min 1800 -16.0 5.0 -40	Min Max 1800 5200 -16.0 16.0 5.0 16.0 1.2 -40 -40 +40 -4.0 4.0 - 20	1800 5200 PPM -16.0 16.0 % 5.0 16.0 sec 1.2 sec -40 +40 % -4.0 4.0 sec - 20 %

TIMING CHARACTERISTICS^(Note 1) (Required -25 °C to +105 °C ambient.)

Notes:

1. Over operating temperature and voltage range unless otherwise noted. Does not include R and C shifts over temperature.

2. Trip point is the frequency in PPM (pulses per minute) that causes the output to change state. An inverted output is low when the speed is greater than the trip point.

3. This is the accuracy required from unit to unit and includes R and C each varying ±5 % over speed, supply voltage, and temperature.

4. Trip point delay is the delay in output response to an input frequency below the trip point. The time delay is determined by the value of the external resistor and capacitor. Delayed version powers up in the passing condition.

5. Passing delay tolerance is based on delay set time. Its tolerance is proportional to delay set time tolerance.

6. Capacitor leakage coefficient is used to calculate leakage current in the following formula: Leakage Current = Leakage Coefficient x Capacitance x Capacitor Voltage

LATCH CHARACTERISTICS^(Note 1) (Required -25 °C to +105 °C ambient.)

Parameter	Min	Max	Unit	Conditions	
Latch Voltage	3.5	4.5	V	At VS = 5.0, Note 2	
C C	2.0	4.5	V		
Latch Current	-	1.0	mA	Note 3	

Notes:

1. Over operating temperature and voltage range unless otherwise noted. External components must be connected between the output and the program/oscillator pin.

2. The open collector output can be used to drive external circuitry that applies a latching voltage to the program/oscillator pin to latch the IC output in the fail state. This latch mode is to be used only on products with delay set times greater than five seconds and with inverted output version of the SSS421L.

3. Latching current is the sourcing current required of the applied external voltage to maintain the latch.

EXTERNAL R AND C CHARACTERISTICS^(Note 1) (Required -25 °C to +105 °C ambient.)

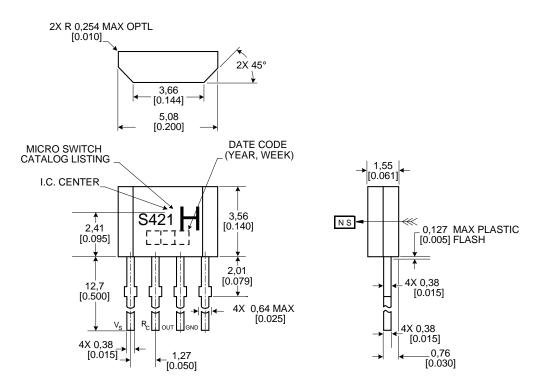
Parameter	Min	Max	Unit	Conditions
External Resistor	-	±5	%	Directly related to Trip Accuracy
External Capacitor	-	±5	%	Directly related to Trip Accuracy
External Capacitor Leakage Coefficient	-	0.05	-	Note 2

Notes:

1. Over operating temperature and voltage range unless otherwise noted.

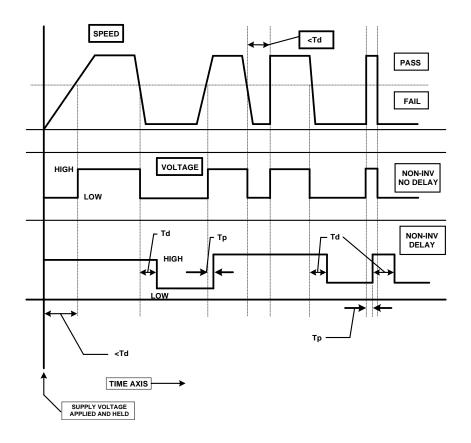
2. Leakage coefficient is the external capacitor leakage current coefficient such that Leakage current = leakage coefficient x capacitance x capacitor voltage.

SS421L/SS421H SERIES MOUNTING DIMENSIONS mm/[in] (for reference only)



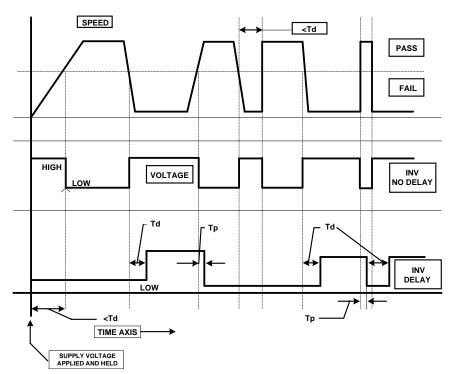
SS421L TIMING DIAGRAM

Td is the time delay after the pulses/min go below the trip point. Td is set by the external RC. Tp is the time delay after the pulses/min go above the trip point. Tp is less than 20% of Td.



SS421H TIMING DIAGRAM

Td is the time delay after the pulses/min go below the trip point. Td is set by the external RC. Tp is the time delay after the pulses/min go above the trip point. Tp is less than 20% of Td



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INTERNET

www.honeywell.com/sensing info.sc@honeywell.com

Honeywell

Sensing and Control www.honeywell.com/sensing Honeywell 11 West Spring Street Freeport, Illinois 61032