AS3711

Quad Buck High Current PMIC with Charger

General Description

The AS3711 is a compact System PMU with integrated battery charger and back light driver.

The device offers advanced power management functions. All necessary ICs and peripherals in a battery powered mobile device are supplied by the AS3711. It features 3 DCDC buck converters as well as 8 low noise LDOs. The different regulated supply voltages are programmable via the serial control interface. 4MHz operation with 1uH coils are reducing cost and PCB space.

AS3711 further features a DCDC buck controller which is ideal to support processor core currents up to 3A.

The two step-up converter generate voltages for e.g.the backlight, classD amplifier, USB host support or LCD display supply. Both constant voltage (for e.g. OLED supply) as well as constant current (white LED backlight) operations with three current sinks are possible. An internal voltage protection is limiting the output voltage in the case of external component failures.

AS3711 contains a linear or switching mode Li-Ion battery charger with constant current and constant voltage. The maximum charging current is 1.5A. An integrated battery switch and an optional external switch are separating the battery during charging or whenever an external power supply is present. With this switch it is also possible to operate with no or deeply discharged batteries. A programmable current limit (100mA - 2.5A) can be used to control the maximum current used from a USB supply or charger input. Additional features are a 30V OV protection and battery temperature supervision.

The single supply voltage may vary from 2.7V to 5.5V.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS3711, Quad Buck High Current PMIC with Charger are listed below:

Figure 1:
Added Value Of Using AS3711

Benefits	Features
Compact design due to small coils for IO and memory voltage generation	• 3 DCDC step down regulators (2-4MHz) - DVM (0.6V-3.3V;1×1.2-1.5A, 2×0.7-1A) - 60µA quiescent current - 2A with combined DCDC 2 & 3
High current generation for processor core	• DCDC step down controller - DVM (0.6V-3.3V; 2-3A)
Supply multiple independent voltage rails for general IO supplies	• 2 analog low noise LDOs, 6 digital LDOs - 2×1.2-3-3V, 6×0.9-3.3V; 150-300mA - 30µA quiescent current (low power mode) • 1 ultra low power always on LDO 2.5V, 10mA
Backlight boost controller for multiple display configurations or fixed voltage supplies	**HV Backlight Driver** • 2×step up with external transistor - e.g. 0.5-1A@5V; 40mA@50V • Voltage control mode and over-voltage protection • 3 programmable current sinks (max. 40mA) • Possible external PWM dimming input (DLS, CABC)
Self contained free configurable charger with stand alone supervisory functions	**Battery Charger** • Programmable trickle charging (25-220mA) • Programmable constant current charging (up to 1500mA) • Programmable constant voltage charging (3.9V-4.25V) • Charger time-out and temperature supervision • Selectable current limitation for USB mode • Integrated battery switch & ideal diode (linear mode) • External battery switch control (switching mode) • External 30V OV protection
Save supervision in HV which works also without a processor	**Supervisor** • Automatic battery monitoring with interrupt generation and selectable warning level • Automatic temperature monitoring with interrupt generation and selectable warning and shutdown levels
Very low current time keeping and alarm functions without the need of a processor	**Real Time Clock** • Ultra low power 32kHz oscillator • Sec and minute counter, auto wake-up • Programmable alarm • Repeating alarm (seconds, minutes, 2 minutes, or 8 minutes) • 32kHz clock output to peripheral • <1µA total power consumption

Benefits	Features
Flexible multi-purpose IOs for general control or measurement tasks	**General Purpose IOs** • 10-bit general purpose ADC input • Wake-up/sleep and DVM input • PWM (DLS, CABC) dimming input • Status output for: charger, low battery, power good and step-up over-current • Q32k clock output • Interrupt output • PWM output • Step-up feedback input
Flexible and fast adaptations to different processors/applications.	**OTP programmable BOOT Sequence** • Programmable regulator default voltages • Programmable start-up sequence
Enables the processor to check the system state in detail	**General Purpose ADC** • 10-bit resolution • Several internal / external sources - VUSB, VSUP, CHGIN, VBAT - GPIOx, CURRx - XOUT32K, SENSEN_SU1, LX_SD4 - Chip temperature
Easy control of all PMIC functions, Safety shutdown feature, without reset button.	**Control Interface** • I^2C control lines, including watchdog • ON input with 4/8s emergency shut-down • Bidirectional reset, with selectable delay • Ultra low power standby mode
No need for external POR or supervisory	**Power-On Reset Circuit**
Dedicated packages for specific applications. Optimization for PCB cost or size.	**Packaging** • QFN56 7×7mm 0.4mm pitch • CSP64 3.6x3.5mm 0.4mm pitch

Applications

The AS3711, Quad Buck High Current PMIC with Charger, is suitable for Portable Media Players, Portable Navigation Devices, E-Books, Mobile Internet Devices, and Tablet PCs.

Figure 2:
AS3711 Block Diagram for QFN56

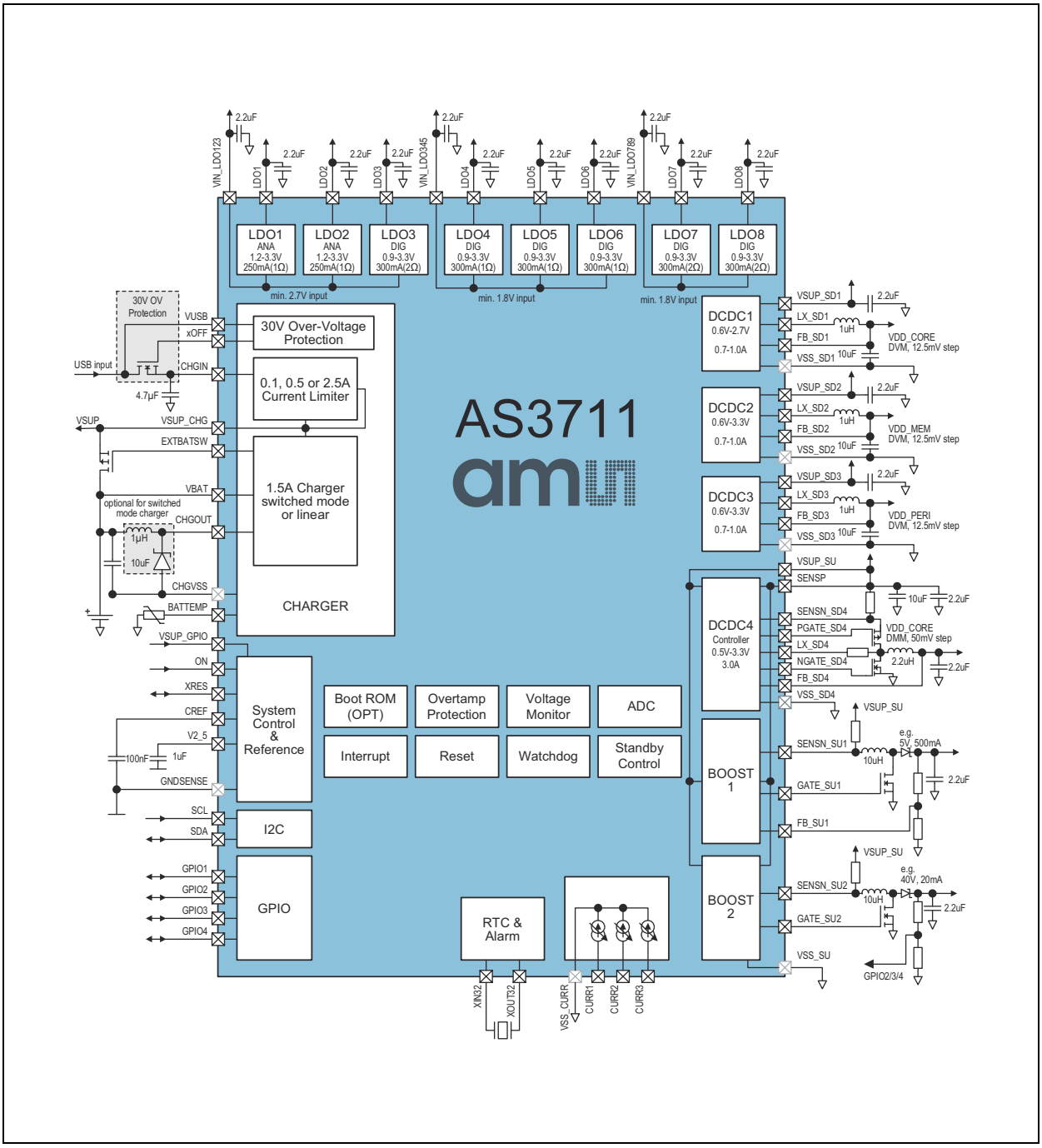
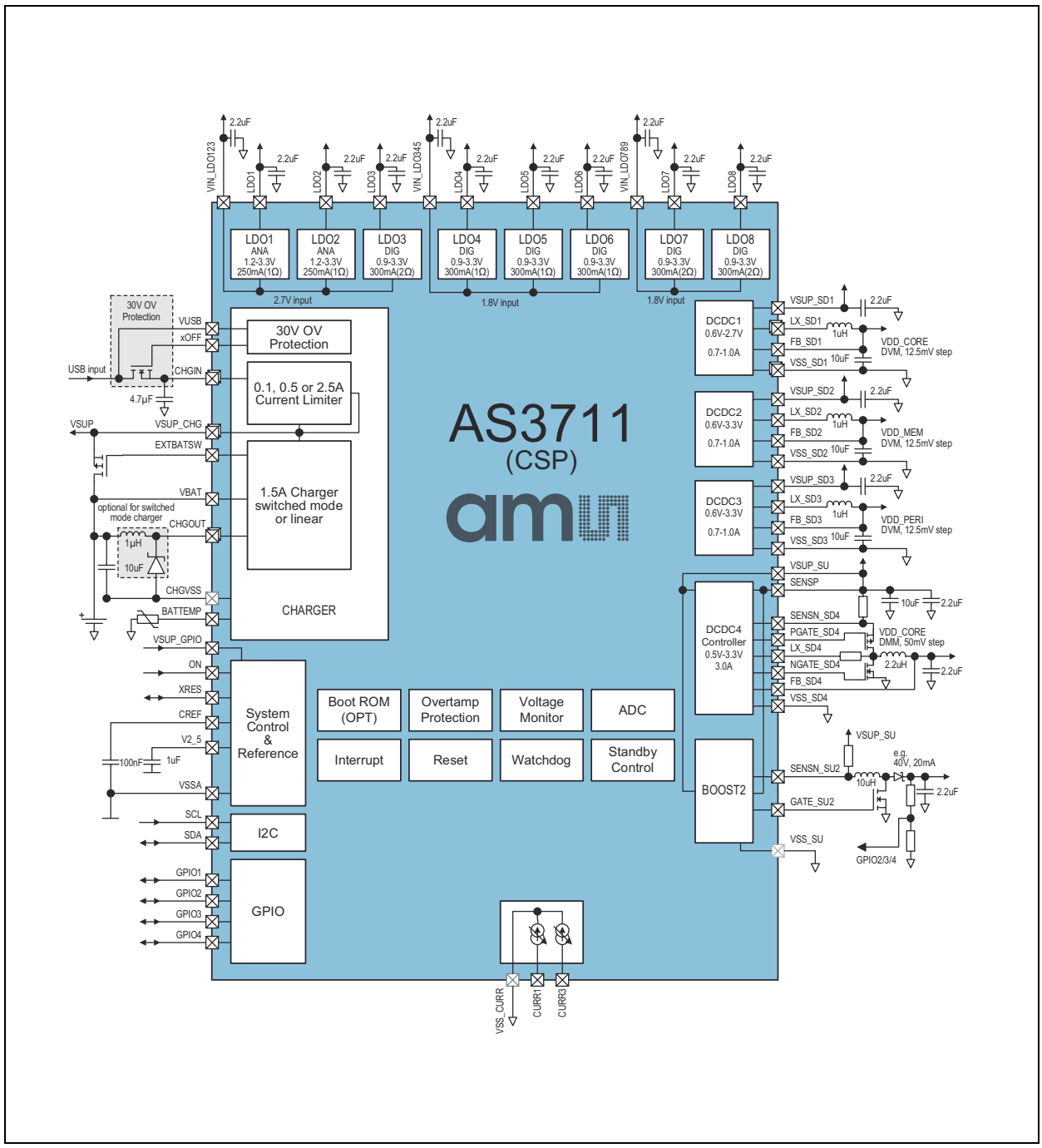


Figure 3:
AS3711 Block Diagram for CSP64



Pin Assignments

Figure 4:
Pin Assignment QFN56 (Top View)

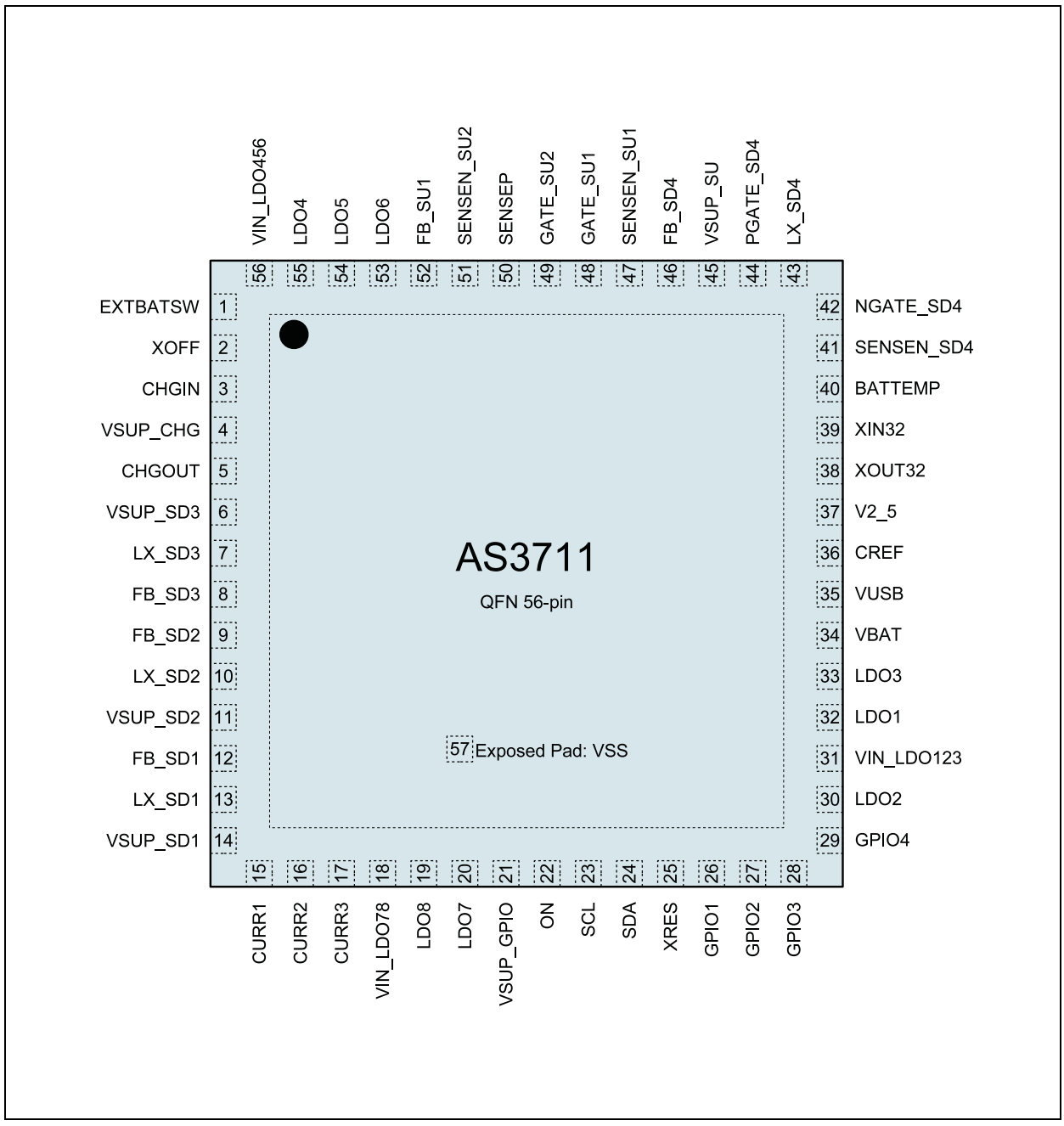


Figure 5:
Ball Assignment CSP64

	1	2	3	4	5	6	7	8
A	LX_SD4	VSS_SSD4	LDO6	LDO5	LDO4	EXTBATSW	CHGIN	CHGIN
B	PGATE_ SD4	FB_SU3	SENSP	VIN_ LDO456	VSSA	XOFF	VSUP_CHG	VSUP_CHG
C	GATE_SU3	VSUP_SU	SENSEN_ SU3	GATE_SU2	VSSA	CHGOUT	CHGOUT	VSUP_SD3
D	BATTEMP	V2_5	CREF	SENSEN_ SU2	GPIO2	FB_SD3	VSS_SD3	LX_SD3
E	VUSB	VBAT	VSSA	GPIO4	XRES	FB_SD2	VSS_SD2	
F	LDO3	LDO1	LDO2	GPIO1	CURR3	FB_SD1	VSUP_SD2	LX_SD2
G	VIN_ LDO123	GPIO3	SDa	ON	VSUP_GPIO	CURR1	VSS_SD1	VSS_SD1
H		SCL	VIN_LDO78	LDO7	LDO8	VSUP_SD1	LX_SD1	LX_SD1

Figure 6:
Pin Descriptions

Pin #		Pin Name	Pin Type	Description	If not used
CSP	QFN	AS3711			
A6	1	EXTBATSW	ANA OUT	External Battery Switch Gate Driver Output	open
B6	2	XOFF	ANA OUT	External OV NMOS Gate Driver Output	open
A7, A8	3	CHGIN	SUP IN	Wall adapter or USB Bus Power Input (after protection)	open
B7, B8	4	VSUP_CHG	SUP IO	Current Limiter Output, Charger Input, connect to VSUPx	always needed
C6, C7	5	CHGOUT	ANA OUT	Linear and DCDC Charger output	open
C8	6	VSUP_SD3	SUP IN	DCDC Step Down 3 Pos. Supply Terminal	always needed
D8	7	LX_SD3	DIG OUT	DCDC Step Down 3 Switch Output to Coil	open
D6	8	FB_SD3	ANA IN	DCDC Step Down 3 Feedback Pin	open
D7	-	VSS_SD3	ANA IO	DCDC Step Down 3 power GND	always needed
E7	-	VSS_SD2	ANA IO	DCDC Step Down 2 power GND	always needed
E6	9	FB_SD2	ANA IN	DCDC Step Down 2 Feedback Pin	open

Pin #		Pin Name	Pin Type	Description	If not used
CSP	QFN	AS3711			
F8	10	LX_SD2	DIG OUT	DCDC Step Down 2 Switch Output to Coil	open
F7	11	VSUP_SD2	SUP IN	DCDC Step Down 2 Pos. Supply Terminal	always needed
F6	12	FB_SD1	ANA IN	DCDC Step Down 1 Feedback Pin	open
G7, G8	-	VSS_SD1	ANA IO	DCDC Step Down 1 power GND	always needed
H7, H8	13	LX_SD1	DIG OUT	DCDC Step Down 1 Switch Output to Coil	open
H6	14	VSUP_SD1	SUP IN	DCDC Step Down 1 Pos. Supply Terminal	always needed
G6	15	CURR1	ANA IO	Load Current Sink 1 Terminal	open
-	16	CURR2	ANA IO	Load Current Sink 2 Terminal	open
F5	17	CURR3	ANA IO	Load Current Sink 3 Terminal	open
H3	18	VINLDO78	SUP IN	LDO 7 & 8 Positive Supply Terminal	always needed
H5	19	LDO8	ANA OUT	LDO8 Output	open
H4	20	LDO7	ANA OUT	LDO7 Output	open
G5	21	VSUP_GPIO	SUP IN	GPIO Positive Supply Terminal, connect to VSUP_CHG	always needed
G4	22	ON	DIG IN	Power Up Input	open
H2	23	SCL	DIG IN	2-wire Serial IF Clock Input	open
G3	24	SDA	DIG IO	2-wire Serial IF Data I/O	open
E5	25	XRES	DIG IO	Reset IO, open-drain (needs external pull-up)	open
F4	26	GPIO1	ANA IO	General Purpose IO 1	open
D5	27	GPIO2	ANA IO	General Purpose IO 2	open
G2	28	GPIO3	ANA IO	General Purpose IO 3	open
E4	29	GPIO4	ANA IO	General Purpose IO 4	open
F3	30	LDO2	ANA OUT	LDO2 Output	open
G1	31	VINLDO123	SUP IN	LDO 1, 2 & 3 Positive Supply Terminal, connect to VSUP_CHG	always needed
F2	32	LDO1	ANA OUT	LDO1 Output	open
F1	33	LDO3	ANA OUT	LDO3 Output	open
E2	34	VBAT	SUP IO	Li-Ion Battery Terminal	open

Pin #		Pin Name	Pin Type	Description	If not used
CSP	QFN	AS3711			
E1	35	VUSB	SUP IN	Wall adapter or USB Bus Power Input (before protection)	open
D3	36	CREF	ANA IO	Reference Bypass Capacitor Terminal	always needed
D2	37	V2_5	ANA OUT	Internal 2.5V Regulator Supply Output	always needed
-	38	XOUT32	ANA OUT	RTC 32kHz Crystal Drive Terminal	open
-	39	XIN32	ANA IN	RTC 32kHz Crystal Feedback Terminal	open
D1	40	BATTEMP	ANA IO	Li-Ion Battery Charger Temperature Sensor Input	open
C3	41	SENSEN_SD4	ANA IN	DCDC Step Down 4 Negative Sense Resistor Input	open
C1	42	NGATE_SD4	ANA OUT	DCDC Step Down 4 ext. NMOS Gate Driver Output	open
A1	43	LX_SD4	ANAIN	DCDC Step Down 4 Sense Input	open
B1	44	PGATE_SD4	ANA OUT	DCDC Step Down 4 ext. PMOS Gate Driver Output	open
A2	-	VSS_SD4	ANA IO	DCDC Step Down 4 power GND	always needed
C2	45	VSUP_SU	SUP IN	DCDC Step Down 4 Positive Supply Terminal, connect to VSUP_CHG	always needed
B2	46	FB_SD4	ANA IN	DCDC Step Down 4 Feedback Pin	open
-	47	SENSEN_SU1	ANA IN	DCDC Step Up 1 Negative Sense Resistor Input	open
-	48	GATE_SU1	ANA OUT	DCDC Step Up 1 ext. NMOS Gate Driver Output	open
C4	49	GATE_SU2	ANA OUT	DCDC Step Up 2 ext. NMOS Gate Driver Output	open
B3	50	SENSEP	ANA IN	DCDC Step Up 1, 2 & Step Down 4 Positive Sense Resistor Input	open
D4	51	SENSEN_SU2	ANA IN	DCDC Step Up 2 Negative Sense Resistor Input	open
-	52	FB_SU1	ANA IN	DCDC Step Up 1 Feedback Pin	open
A3	53	LDO6	ANA OUT	LDO6 Output	open

Pin #		Pin Name	Pin Type	Description	If not used
CSP	QFN	AS3711			
A4	54	LDO5	ANA OUT	LDO5 Output	open
A5	55	LDO4	ANA OUT	LDO4 Output	open
B4	56	VINLDO456	SUP IN	LDO 4, 5 & 6 Positive Supply Terminal	always needed
B5, C5, E3	-	VSSA	ANA IO	Analog GND input	always needed

Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 7:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
	5V pins	-0.5	7.0	V	Applicable for pins VSUP_CHG, VSUP_SD1/2/3, VSUP_SU, VSUP_GPIO, VIN_LDO123/456/78, GPIO1/2/3/4, GATE_SU1/2, NGATE_SD4, PGATE_SD4, FB_SU1, SENSEP, SENSEN_SU1/2, SENSEN_SD4, VBAT, LDO1/2/3/4/5/6/7/8, FB_SD1/2/ 3/4, LX_SD1/2/3/4, XRES, SCL, SDA
	3V pins	-0.5	5.0	V	Applicable for pins V2_5, CREF, ON, BATTEMP, XIN32, XOUT32
	30V pins	-0.5	32	V	Applicable for pin VUSB, XOFF, CURR1/2/3
I_{SCR}	Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC JESD78
Continuous Power Dissipation (T_A = +70°C)					
P_T	Continuous power dissipation		1.4	W	P_T [(1)] for CSP64 package (R_{TH} ~ 40K/W)
			1.8	W	P_T [(1)] for QFN56 package (R_{TH} ~ 30K/W)
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM		±1.5	kV	Norm: JEDEC JESD22-A114F
Temperature Ranges and Storage Conditions					
T_{AMB}	Operating Temperature	-40	+85	°C	
T_J	Junction Temperature		+125	°C	for CSP64 package
			+150	°C	for QFN56 package
T_{STRG}	Storage Temperature Range	-55	+150	°C	

Symbol	Parameter	Min	Max	Units	Comments
T_{BODY}	Package Body Temperature		260	°C	Norm IPC/JEDEC J-STD-020 (2) For QFN, the lead finish for Pb-free leaded packages is matte tin (100% Sn)
RH_{NC}	Humidity non-condensing	5	85	%	
MSL	Moisture Sensitive Level	1			For CSP64, represents an unlimited max. floor live time
		3			For QFN56, represents a max. floor life time of 168h

Note(s) and/or Footnote(s):

1. Depending on actual PCB layout and PCB used.
2. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices".

Electrical Characteristics

VSUPx=+2.7V to +5.5V, T_A =-40°C to +85°C. Typical values are at VSUPx=+3.6V, T_A=+25°C, unless otherwise specified.

The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 8:
Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VUSB	Charger HV Input		0	5	30	V
CHGIN	Charger LV Input		0	5	5.5	V
VSUPx	Supply Voltage VSUP_x		2.7	3.6	5.5	V
VINLDO123	Supply Voltage for LDO 1, 2 & 3		2.7	3.6	5.5	V
VINLDO456	Supply Voltage for LDO 4, 5 & 6		1.8	3.6	5.5	V
VINLDO78	Supply Voltage for LDO 7 & 8		1.8	3.6	5.5	V
V2_5	Voltage on Pin V2_5		2.4	2.5	2.6	V
I_{low_power}	Low Power current	@ VSUPx = 4.2V		220		µA
I_{power_off}	Power-Off current	All regulators OFF V2_5 ON		10		µA

Typical Operating Characteristics

Please see operating characteristics in the block description chapters.

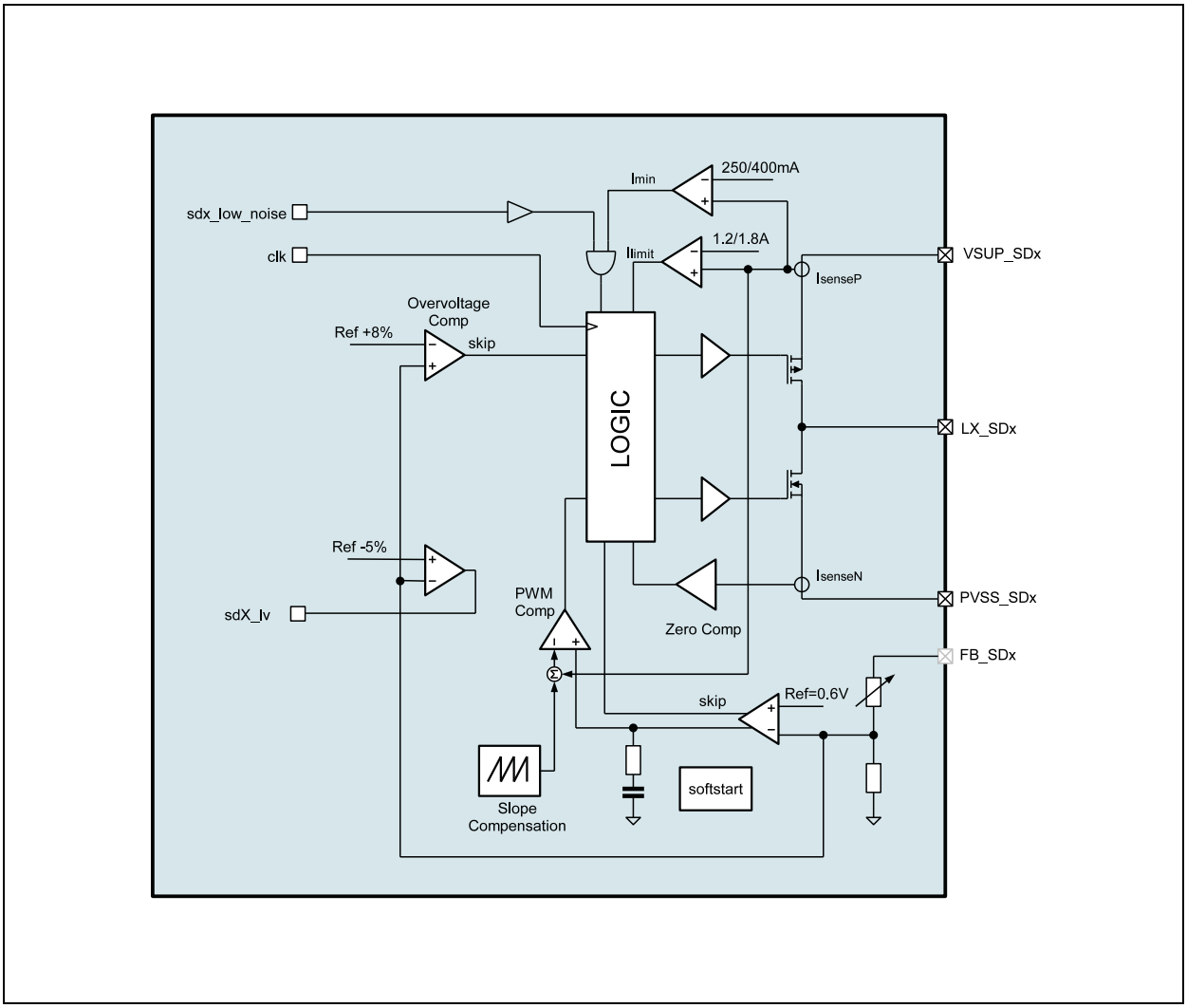
Detailed Description - Power Management Functions

DCDC Step-Down Converter

Description

The step-down converter is a high efficiency fixed frequency current mode regulator. By using low resistance internal PMOS and NMOS switches efficiency up to 95% can be achieved. The fast switching frequency allows using small inductors, without increasing the current ripple. The unique feedback and regulation circuit guarantees optimum load and line regulation over the whole output voltage range, up to an output current of 1A (SD2, SD3) and 1.5A for SD1, with an output capacitor of only 10µF. The implemented current limitation protects the DCDC and the coil during overload condition.

Figure 9:
Step Down DC/DC Converter Block diagram



Mode Settings

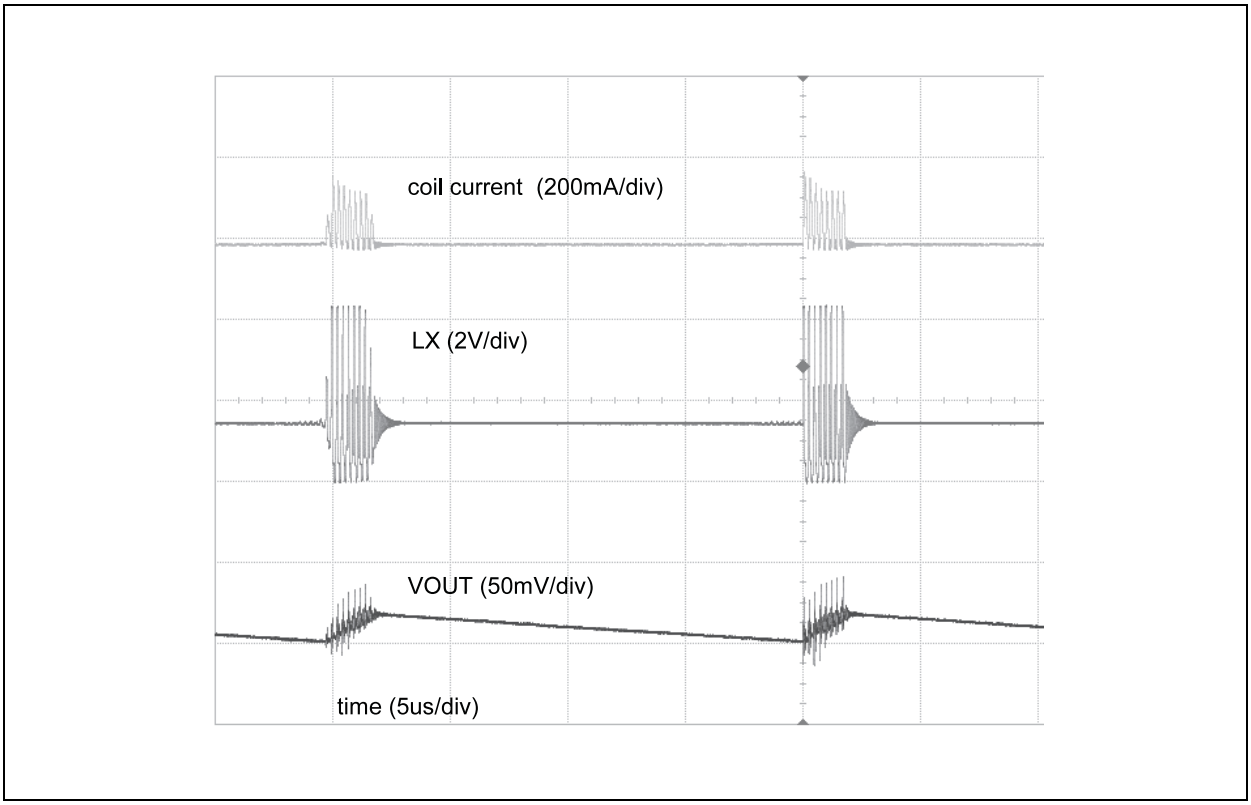
Low ripple, low noise operation:

Bit settings: sdX_low_noise=1

In this mode there is no minimum coil current necessary before switching OFF the PMOS. As long as the load current is superior to the ripple current the device operates in continuous mode. When the load current gets lower, the discontinuous mode is triggered. As result, the auto-zero comparator stops the NMOS conduction to avoid load discharger and the duty cycle is reduced down to tmin_on to keep the regulation loop stable. This results in a very low ripple and noise, but decreased efficiency, at light loads, especially at low input to output voltage differences.

Only in the case the load current gets so small that less than the minimum ON-time of the PMOS would be needed to keep the loop in regulation the regulator will enter low power mode operation. The crossover point is about 15mA for Vin=3V, Vout=1.2V, 1uH, 4MHz.

Figure 10:
DCDC Buck with enabled Low Noise Mode



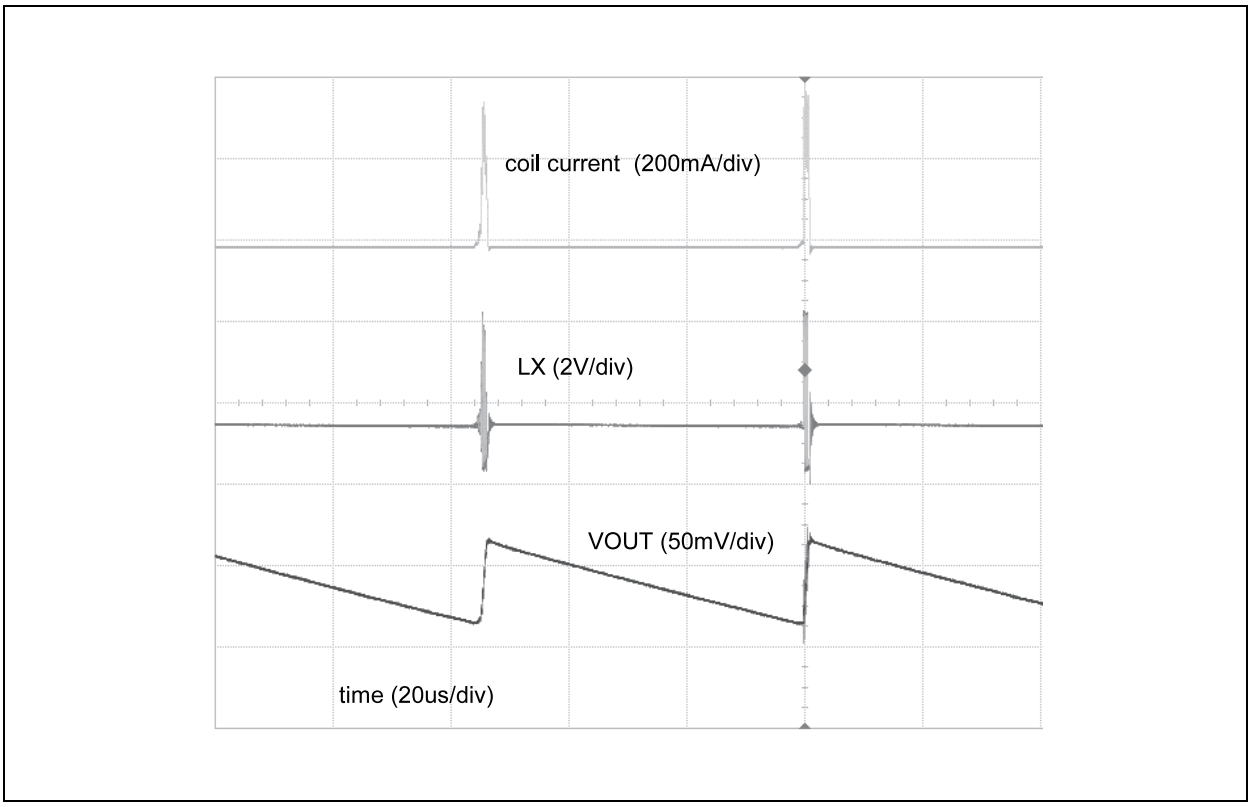
High efficiency operation (default setting):

Bit settings: sdX_low_noise=0

In this mode there is a minimum coil current necessary before switching OFF the PMOS. As a result there are less pulses necessary at low output loads, and therefore the efficiency at low output load is increased. As drawback this mode increases the ripple up to a higher output currents.

The crossover point to low power mode is already reached at reasonable high output currents. (e.g. @110mA for Vin=3V, Vout=1.2V, 1uH, 4MHz)

Figure 11:
DCDC Buck with disabled Low Noise Mode



It's possible to switch between these two modes during operation:

Low power mode operation (automatically controlled):

As soon as the output voltage stays above the desired target value for a certain time, some internal blocks will be powered down leaving the output floating to lower the power consumption. Normal operation starts as soon as the output drops below the target value for a similar amount of time. To minimize the accuracy error some internal circuits are kept powered to assure a minimized output voltage ripple.

Two addition guard bands, based on comparators, are set at ±5% of the target value to react quickly on large over/undershoots by immediately turning on the output drivers without the normal time delays. This ensures a minimized ripple also in very extreme load conditions.

DVM (Dynamic Voltage Management)

To minimize the over-/undershoot during a change of the output voltage, the DVM can be enabled. With DVM the output voltage will ramp up/down with a selectable slope after the new value was written to the registers. Without DVM the slew rate of the output voltage is only determined by external components like the coil and load capacitor as well as the load current.

DVM can be selected for all step-down converters, but only for one at a time. (see sd_dvm_select and dvm_time description)

Fast Regulation Mode

This mode can be used to react faster on sudden load changes and thus minimize the over-/undershoot of the output voltage. This mode needs an 22uF output capacitor instead the 10uF one to guarantee the stability of the regulator. The mode is enabled by setting sdX_fast =1.

Selectable Frequency Operation

Especially for very low load conditions, e.g. during a sleep mode of a processor, the switching frequency can be reduced to achieve a higher efficiency. The frequency for SD1, SD2 and SD3 can be set to 2, 3 or 4MHz. This mode is selected by setting sdX_freq and sdX_fsel to the appropriate values.

100% PMOS ON Mode for Low Dropout Regulation

For low input to output voltage difference the DCDC converter can use 100% duty cycle for the PMOS transistor, which is then in LDO mode.

Step-Down Converter Configuration Modes

The step down DCDC converters have two configuration modes to deliver different output currents for the applications. The operating mode is selected by setting the bit sd3_slave (the default is set by the Boot-OTP).

Figure 12:
DC/DC step-down SD1, SD2, SD3 Normal Operating Mode; sd3_slave = 0

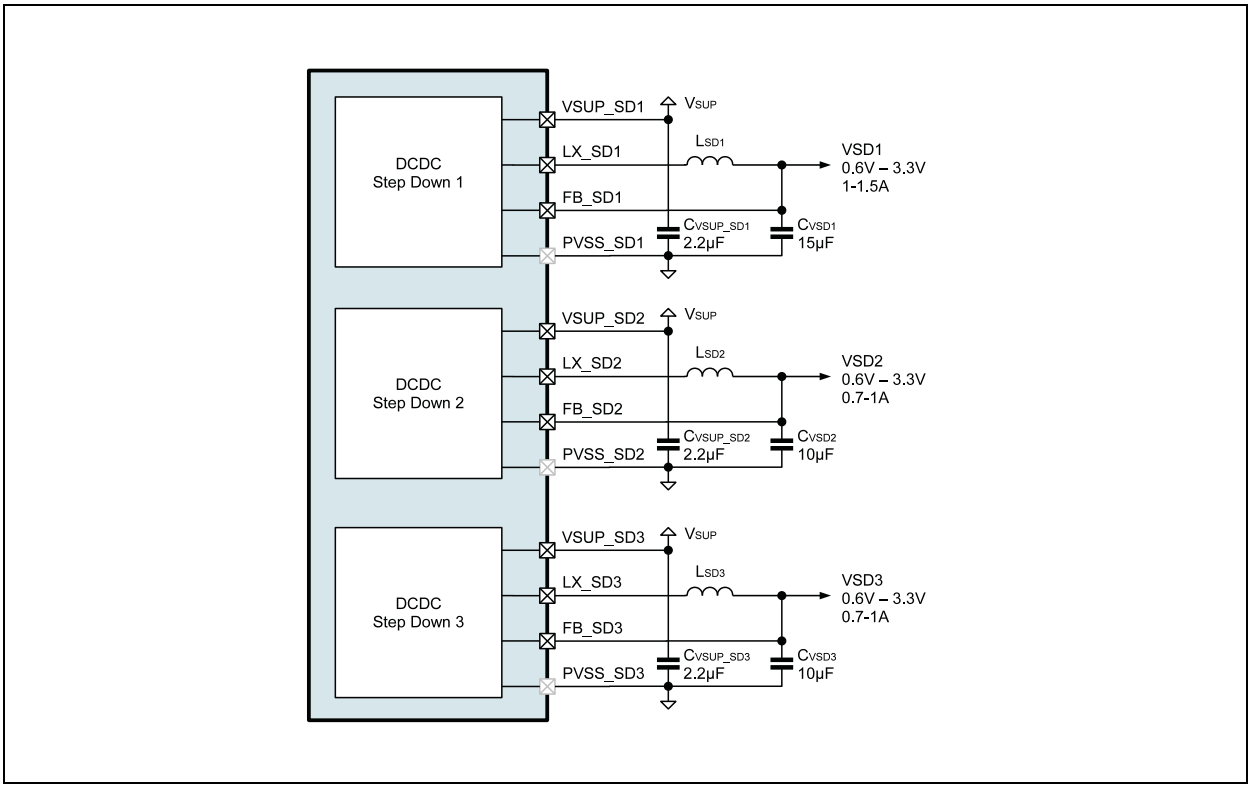
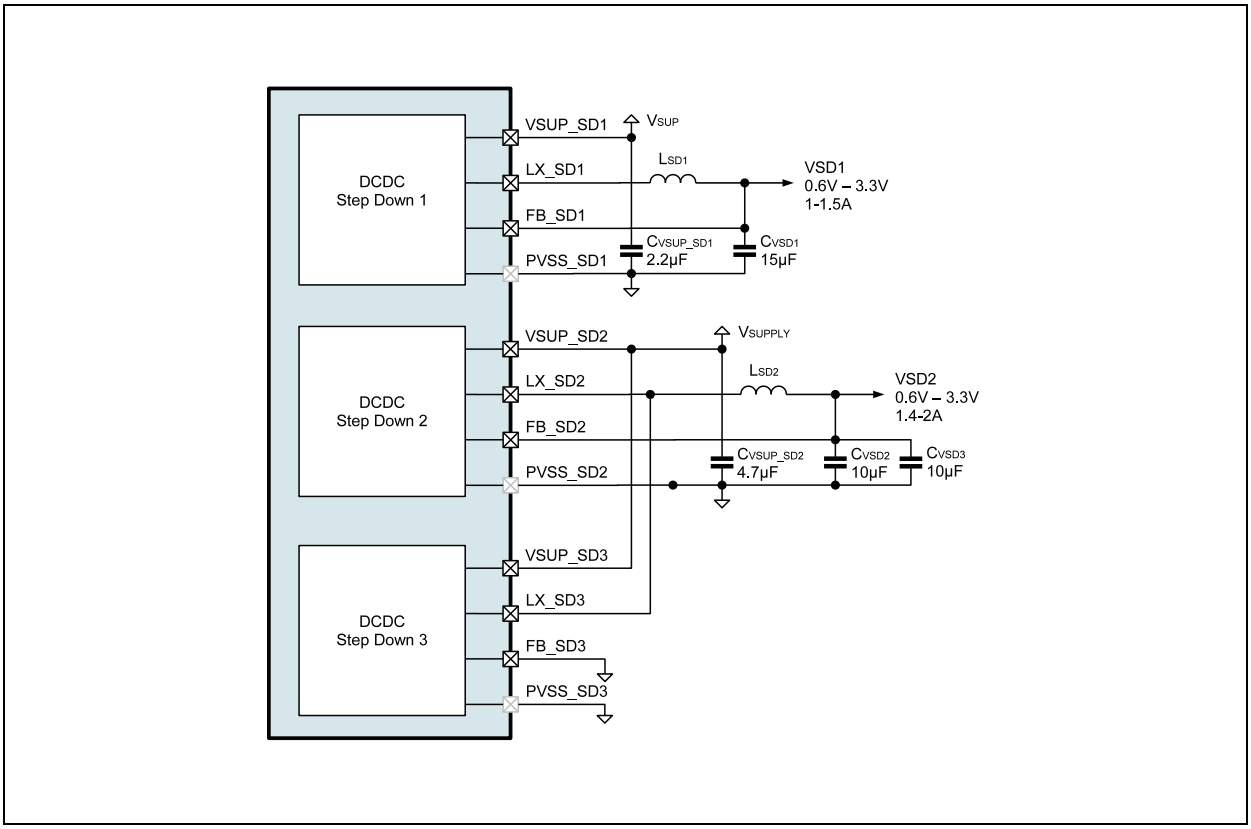


Figure 13:
DC/DC step-down SD1, SD2, SD3 2A Operating Mode; sd3_slave = 1



Parameter

Figure 14:
Step Down DC/DC Converter Parameters

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{IN}	Input voltage	Pin VSUP_SDx	2.7		5.5	V
V_{OUT}	Regulated output voltage		0.6125		3.35	V
VOUT_tol	Output voltage tolerance	min. 40mV	-3		+3	%
I_{LIMIT}	Current limit	SD1		1.8		A
		SD2, SD3		1.2		A
RPSW	P-Switch ON resistance	SD1; VSUP_SDx=3.0V		0.17	0.4	Ω
		SD2, SD3; VSUP_SDx=3.0V		0.25	0.5	Ω
RNSW	N-Switch ON resistance	SD1; VSUP_SDx=3.0V		0.17	0.4	Ω
		SD2, SD3; VSUP_SDx=3.0V		0.25	0.5	Ω
I_{Load}	Load current	SD1	0		1.5	A
		SD2, SD3	0		1	A
f_{SW}	Switching frequency	sdX_frequ=1, sdX_fsel=1; fclk_int =4MHz		4		MHz
		sdX_frequ=1, sdX_fsel=0; fclk_int =4MHz		3		MHz
		sdX_frequ=0, sdX_fsel=0; fclk_int =4MHz		2		MHz
tmin_on	Minimum ON time			40		ns
ηeff	Efficiency	Iout=300mA, Vout=2V, VSUP=3.5V		92		%
I_{VDD}	Current consumption	Operating current without load		60		µA
		Shutdown current		0.1		

Figure 15:
Step Down DC/DC External Components

Symbol	Parameter	Note	Min	Typ	Max	Unit
C_{FB_SD1}	Output capacitor	Ceramic X5R or X7R	10.0	15		µF
		Ceramic X5R or X7R, fast mode=1	20.0	30		µF
C_{FB_SD2-3}	Output capacitor	Ceramic X5R or X7R	8.0	10		µF
		Ceramic X5R or X7R, fast mode=1	16.0	20		µF
C_{VSUP_SD1-3}	Input capacitor	Ceramic X5R or X7R		2.2		µF
$L_{SD1-SD3}$	Inductor	4MHz operation		1		µH
		3MHz operation		1		
		2MHz operation		2.2		

All measurements where done with 55mΩ chip coils (Murata LQM2HPN1R0MG0). Using coils with lower on-resistance will increase the efficiency especially at higher output currents.

Figure 16:
Step Down DC/DC SD1 Efficiency vs. Output Current; V_{SUP} = 3.0V, 3MHz operation, T_A = +25°C

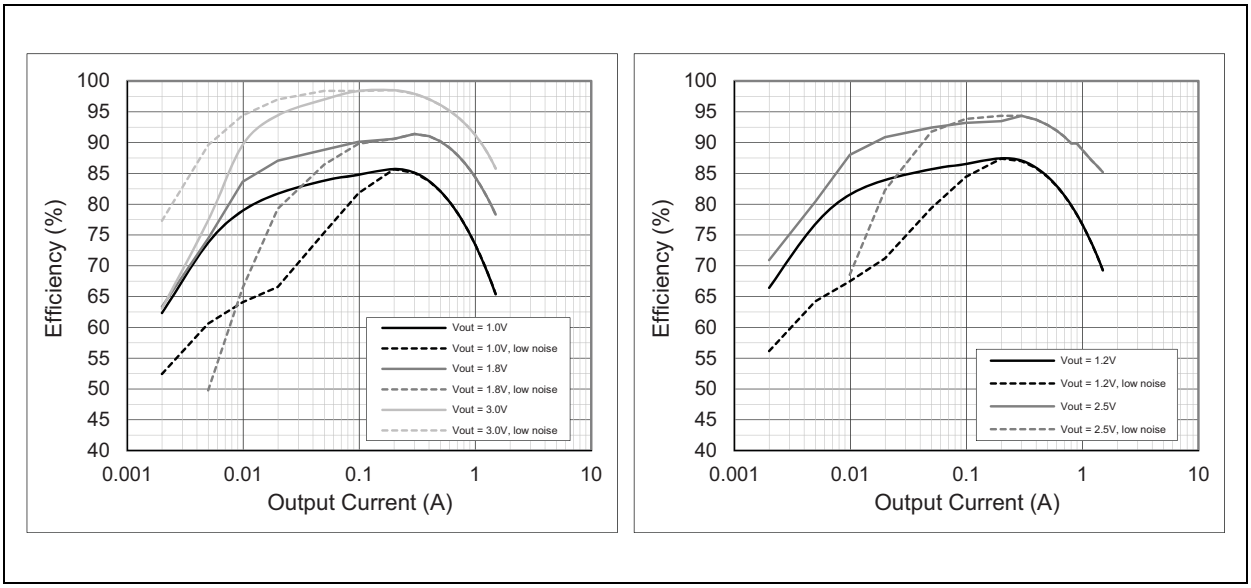


Figure 17:
Step Down DC/DC SD1 Efficiency vs. Output Current; V_{SUP} = 3.8V, 3MHz operation, T_A = +25°C

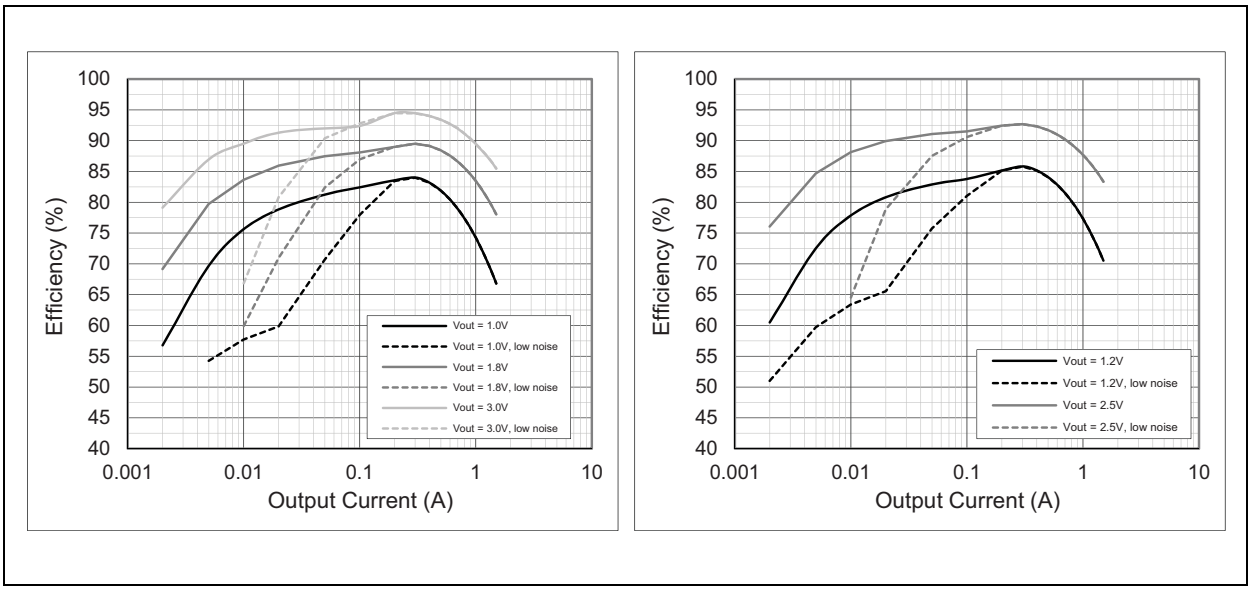


Figure 18:
Step Down DC/DC SD2 & SD3 Efficiency vs. Output Current; V_{SUP} = 3.0V, 3MHz operation, T_A = +25°C

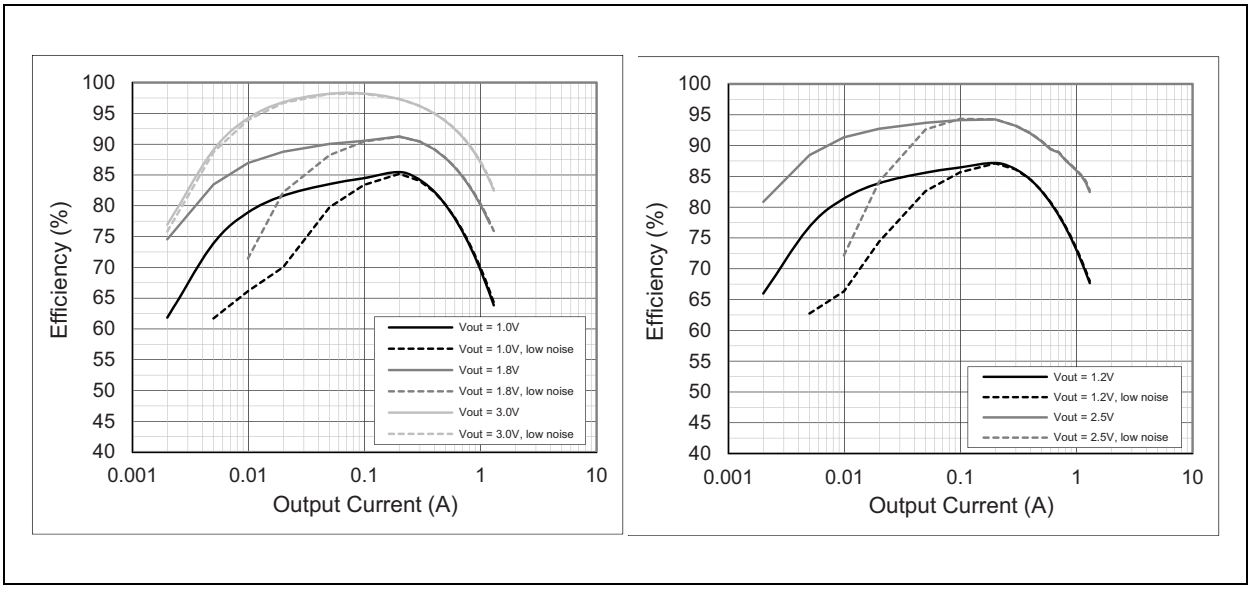
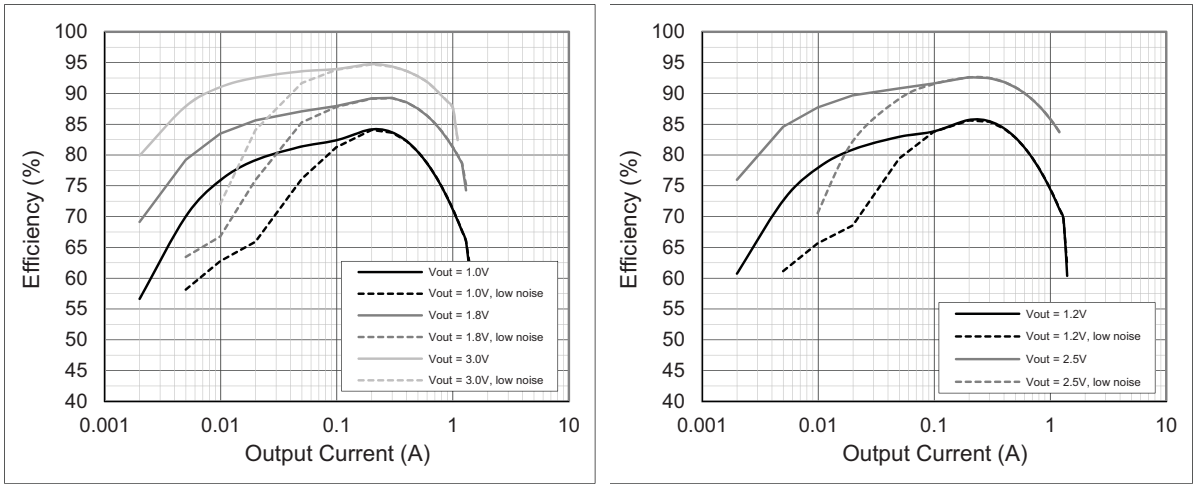


Figure 19:
Step Down DC/DC SD2 & SD3 Efficiency vs. Output Current; V_{SUP} = 3.8V, 3MHz operation, T_A = +25°C

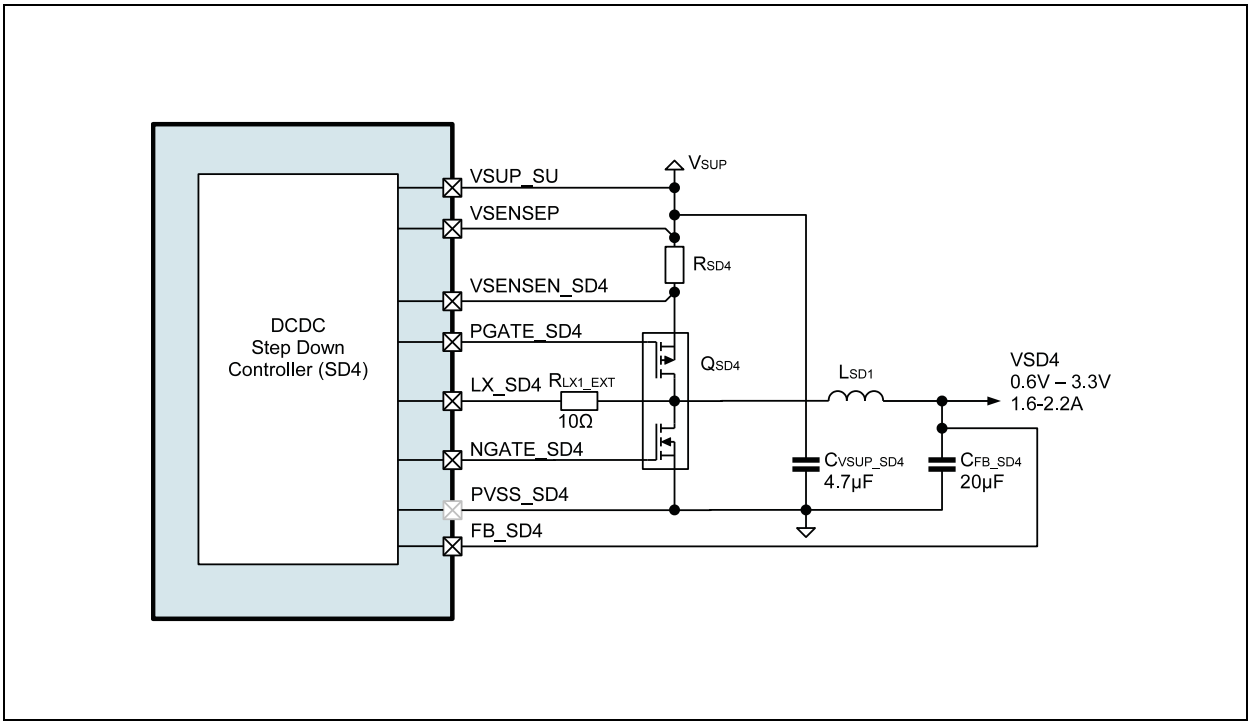


DCDC Step-Down Controller

Description

The Step-Down controller SD4 uses a paired external NMOS, PMOS to achieve higher output currents. the maximum output current is determined by the external transistor and shunt used.

Figure 20:
DC/DC step-down Controller



Parameter

Figure 21:
Step Down DC/DC Controller Parameters

Symbol	Parameter	Note	Min	Typ	Max	Unit
VIN	Input voltage	Pin VSUP_SDx	2.7		5.5	V
VOUT	Regulated output voltage		0.6125		3.3	V
VOUT_tol	Output voltage tolerance	min. 40mV	-3		+3	%
V_{rsense_max}	Current limit voltage at Rsense	E.g.: 2.6A for 0.033Ω sense resistor		100		mV
f_{SW}	Switching frequency	fclk_int = 4MHz		1		MHz

Figure 22:
Step Down DC/DC Controller External Components

Symbol	Parameter	Note	Min	Typ	Max	Unit
External Components 1.6A						
Q_{SD4}	Paired NMOS-PMOS	FDC6327C	PMOS: Ron=250mOhm, 1.6A NMOS: Ron=120mOhm, 2.7A			
R_{SD4}	Shunt	0.15W; ±1%		50		mΩ
C_{FB_SD4}	Output capacitor	Ceramic X5R or X7R	16.0	20		µF
		Ceramic X5R or X7R, fast mode=1	32.0	40		µF
C_{VSUP_SD4}	Input capacitor	Ceramic X5R or X7R		10		µF
L_{SD4}	Inductor	2A rated, 1MHz operation		2.2		µH
External Components 2.2A						
Q_{SD4}	Paired NMOS-PMOS	FDC6420C	PMOS: Ron=190mOhm, 2.2A NMOS: Ron=95mOhm, 3A			
R_{SD4}	Shunt	0.2W; ±1%		33		mΩ
C_{FB_SD4}	Output capacitor	Ceramic X5R or X7R	24.0	30		µF
		Ceramic X5R or X7R, fast mode=1	48.0	60		µF
C_{VSUP_SU}	Input capacitor	Ceramic X5R or X7R		10		µF
L_{SD4}	Inductor	2.5A rated, 1MHz operation		1.5		µH

Symbol	Parameter	Note	Min	Typ	Max	Unit
External Components 3A						
Q_{SD4}	paired NMOS-PMOS	NTHD3102C	PMOS: Ron=83mOhm, 4.2A NMOS: Ron=37mOhm, 5.5A			
R_{SD4}	Shunt	0.3W; ±1%		25		mΩ
C_{FB_SD4}	Output capacitor	Ceramic X5R or X7R	32.0	40		µF
		Ceramic X5R or X7R, fast mode =1	64.0	80		µF
C_{VSUP_SU}	Input capacitor	Ceramic X5R or X7R		10		µF
L_{SD4}	Inductor	3A rated, 1MHz operation		1		µH

All measurements where done with the 2.2A transistors (Fairchild FDC6420C) and 70mΩ chip coils (Murata LQM2HPN1R0MG0). Using coils with lower on-resistance will increase the efficiency especially at higher output currents.

Figure 23:
Step-Down DC/DC SD4 Controller Efficiency vs. Output Current; V_{SUP} = 3.0V, T_A = +25°C

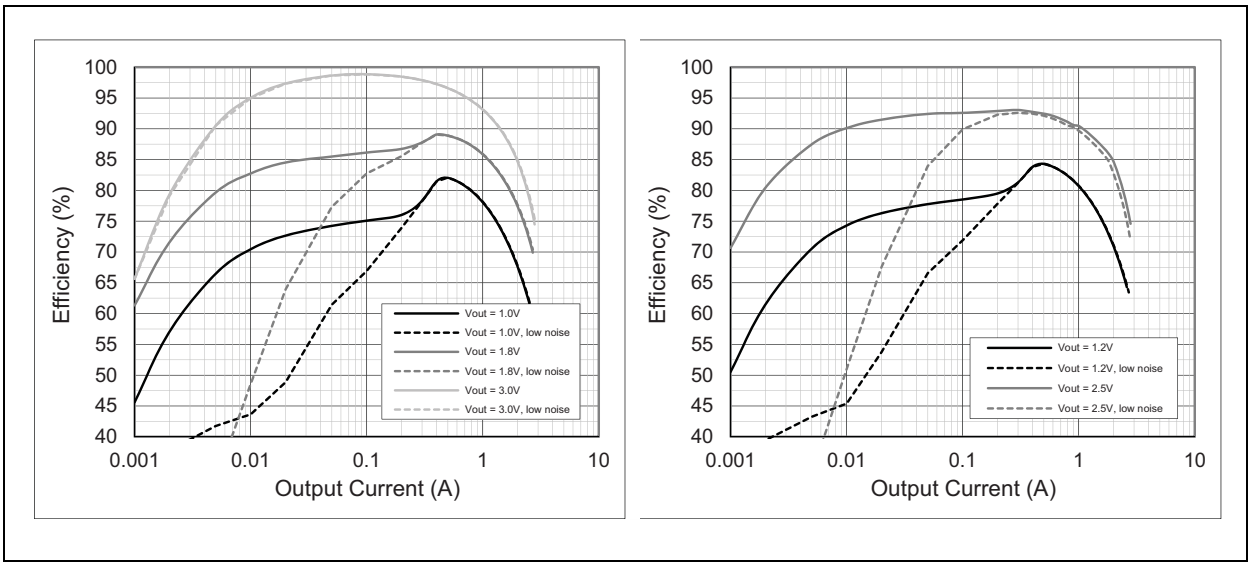
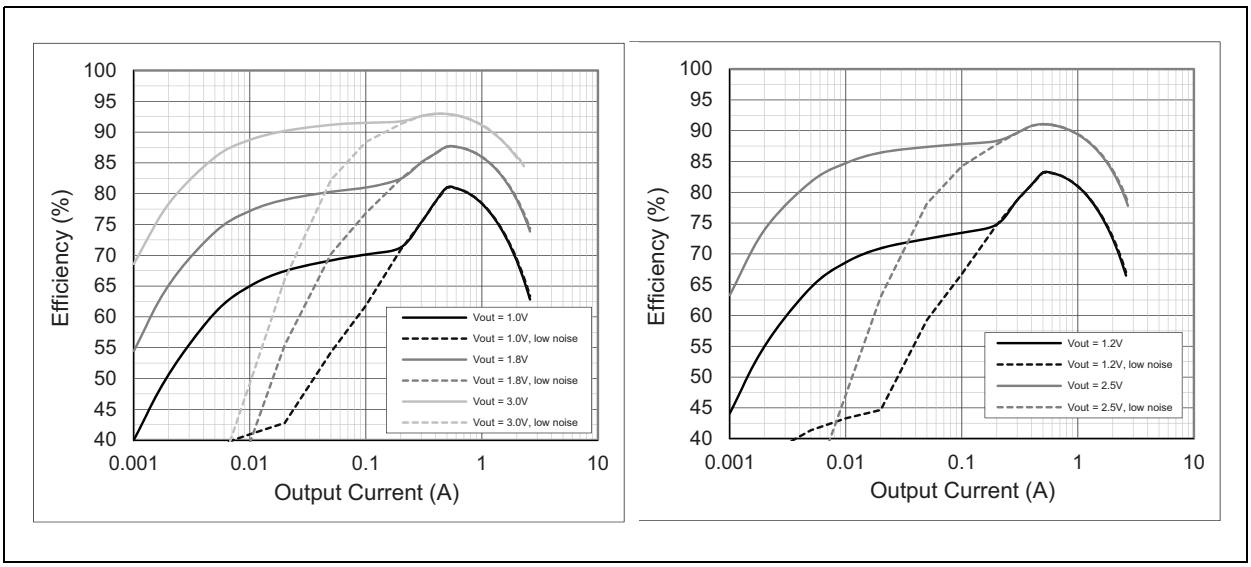


Figure 24:
Step-Down DC/DC SD4 Controller Efficiency vs. Output Current; V_{SUP} = 3.8V, T_A = +25°C



Analog LDO Regulators

Description

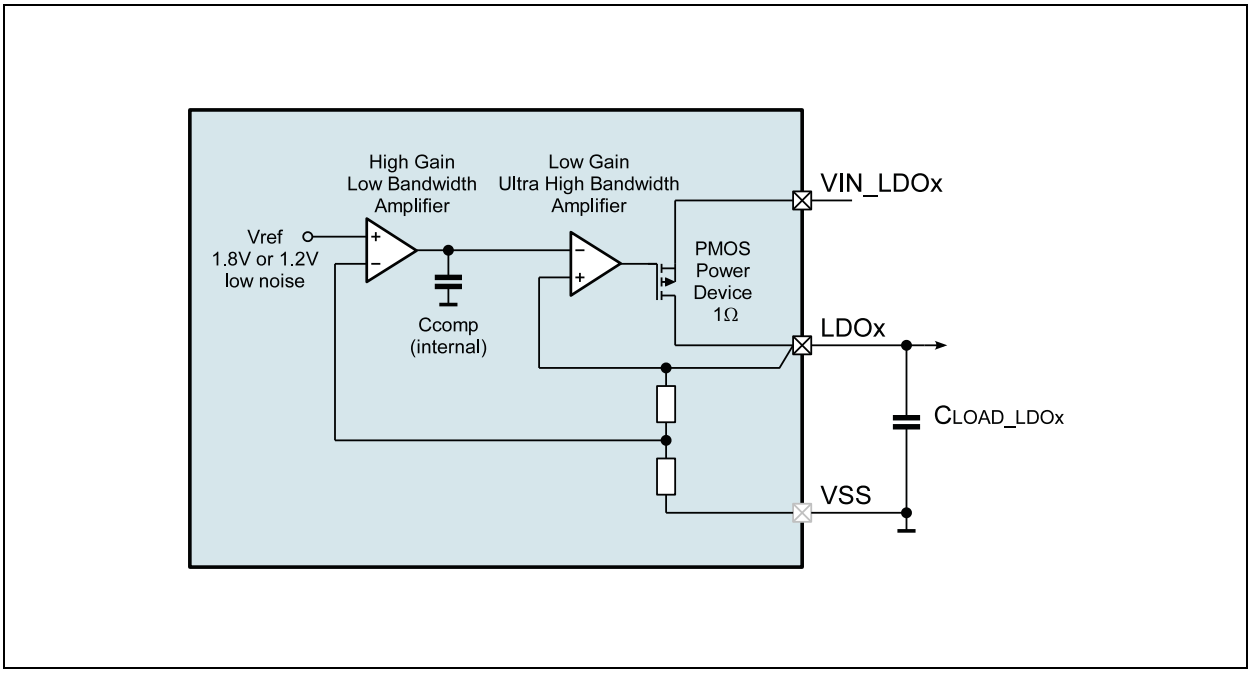
LDO1 and LDO2 are designed to supply sensitive analogue circuits like LNA's, Transceivers, VCO's and other critical RF components of cellular radios. Another application is the supply of audio devices or as a reference for AD and DA converters. The design is optimized to deliver the best compromise between quiescent current and regulator performance for battery powered devices.

Stability is guaranteed with ceramic output capacitors of 1µF ±20% (X5R) or 2.2µF +100/-50% (Z5U). The low ESR of these caps ensures low output impedance at high frequencies. Regulation performance is excellent even under low dropout conditions, when the power transistor has to operate in linear mode. Power supply rejection is high enough to suppress the PA-ripple on the battery in TDMA systems at the output. The low noise performance allows direct connection of noise sensitive circuits without additional filtering networks. The low impedance of the power device enables the device to deliver up to IOUT current even at nearly discharged batteries without any decrease of performance.

The default guaranteed operating current during start-up is 150mA, but can be set to 250mA with ldoX_ilimit = 1.

To save power in low-power states where the full performance is not needed the bias current can be reduce by setting reg_low_bias_mode=1.

Figure 25:
Analog LDO Block Diagram



Parameter

Figure 26:
Analog LDO (LDO1, LDO2) Characteristics
VLDO123_IN=3.7V; ILOAD=150mA; T_{AMB}=25°C; CLOAD =2.2µF (Ceramic); unless otherwise specified

Symbol	Parameter	Note	Min	Typ	Max	Unit
VLDO123_IN	Supply voltage range		2.7		5.5	V
I_{OUT}	Output current (1)	ldoX_ilimit = 0	0		150	mA
		ldoX_ilimit = 1	0		250	
R_{ON}	On resistance	LDO1, LDO2			1	Ω
PSRR	Power supply rejection ratio	f=1kHz	70			dB
		f=100kHz	40			
I_{OFF}	Shut down current				100	nA
I_{VDD}	Supply current	Without load		50		µA
		Without load, reg_low_bias_mode=1		30		µA
Noise	Output noise	10Hz < f < 100kHz			50	μV_{rms}
t_{start}	Startup time	low current limit used during start-up			200	µs
V_{out}	Output voltage		1.2		3.3	V
Vout_tol	Output voltage tolerance	min. 40mV	-3		3	%
$V_{LineReg}$	Line regulation	Static	-1		1	mV
		Transient; Slope: t_r=10µs	-10		10	
$V_{LoadReg}$	Load regulation	Static	-1		1	mV
		Transient; Slope: t_r=10µs	-10		10	
$I_{LIMIT\_LDO1,2\_L}$	Low current limit	ldoX_ilimit = 0		300		mA
$I_{LIMIT\_LDO1,2\_H}$	High current limit	ldoX_ilimit = 1		500		mA
$C_{LOAD\_LDO1,2\_L}$	Ceramic load capacitor	LDO1 / LDO2; ldoX_ilimit = 0	1		5	µF
$C_{LOAD\_LDO1,2\_H}$	Ceramic load capacitor	LDO1 / LDO2; ldoX_ilimit = 1	2		5	µF

Note(s) and/or Footnote(s):

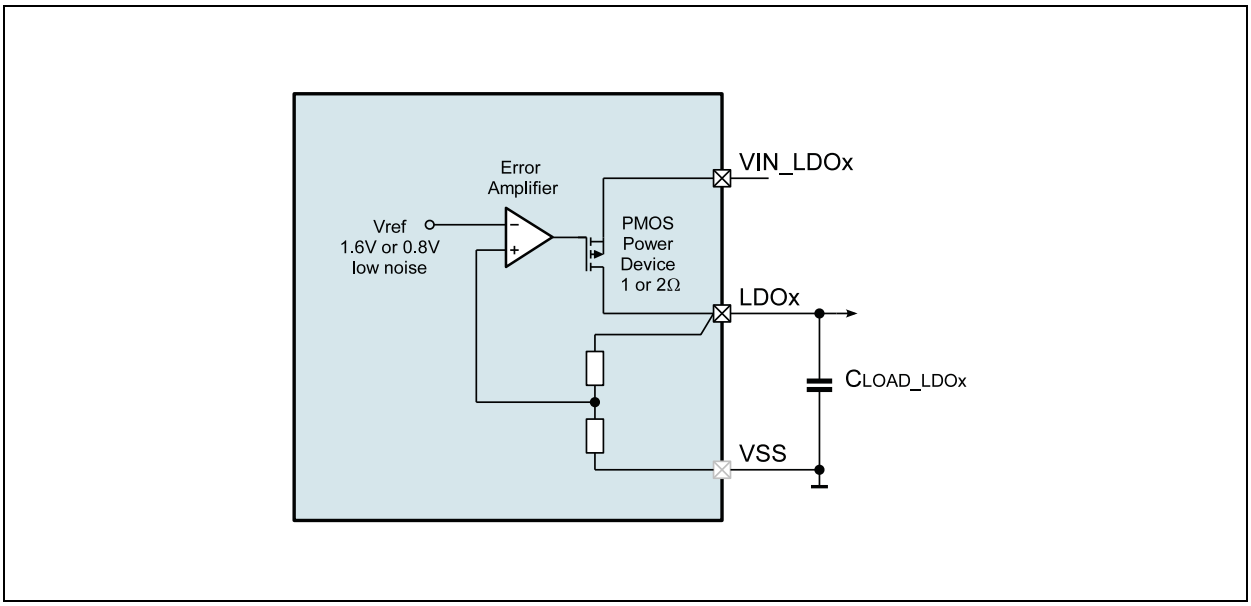
1. Guaranteed by design and verified by laboratory evaluation and characterization; not production tested.

Digital LDO Regulators

Description

Digital LDOs offer a wide input (1.8V to 5.5V) as well as a wide output (0.9 to 3.3V) voltage range to be used for general purpose peripheral supply. Up to 300mA possible output currents are offered with good noise and regulation performance and very low quiescent current even suitable for stand-by power supply.

Figure 27:
Digital LDO Block diagram



Parameter

Figure 28:
Digital LDO (LDO3, LDO4, LDO5, LDO6, LDO7, LDO8) Characteristics
VLDOx_IN=3.7V; ILOAD=150mA; Tamb=25°C; CLOAD =1µF (Ceramic); unless otherwise specified

Symbol	Parameter	Note	Min	Typ	Max	Unit
VLDO123_IN	Supply voltage range		2.7		5.5	V
VLDO456_IN	Supply voltage range		1.75		5.5	V
VLDO78_IN	Supply voltage range		1.75		5.5	V
IOUT	Output current (1)	ldoX_ilimit = 0	0		150	mA
		ldoX_ilimit = 1	0		300	mA
RON	On resistance	LDO4, LDO5, LDO6			1	Ω
		LDO3, LDO7, LDO8			2	Ω

Symbol	Parameter	Note	Min	Typ	Max	Unit
PSRR	Power supply rejection ratio	f=1kHz	60			dB
		f=100kHz	30			
IOFF	Shut down current			100		nA
IVDD	Supply current	Without load		30	43	µA
tstart	Startup time	Low current used during start-up			200	µs
Vout	Output voltage	Vsupply>3.0V, VCP=5.2V, Iout<200mA	0.9		3.3	V
Vout_tol	Output voltage tolerance	min. 40mV	-3		3	%
VLineReg	Line regulation	Static		0.07		%/V
		Transient; Slope: tr=15µs; delta 1V		20		mV
VLoadReg	Load regulation	Static		0.014		%/mA
		Transient; Slope: tr=15µs; 1mA->300mA		30		mV
ILIMIT_LDO3-8_L	Low current limit	ldoX_ilimit = 0		300		mA
ILIMIT_LDO3-8_H	High current limit	ldoX_ilimit = 1		500		mA
$C_{LOAD\_LDO3-8\_L}$	Ceramic load capacitor	LDO1 / LDO2; ldoX_ilimit = 0	1		5	µF
$C_{LOAD\_LDO3-8\_H}$	Ceramic load capacitor	LDO1 / LDO2; ldoX_ilimit = 1	2		5	µF

Note(s) and/or Footnote(s):

1. Guaranteed by design and verified by laboratory evaluation and characterization; not production tested.

Low power LDO V2_5 Regulators

Description

The low power LDO V2_5 is needed to supply the chip core (analog and digital) of the device. It is designed to get the lowest possible power consumption, and still offering reasonable regulation characteristics. The regulator has two supply inputs selecting automatically the higher one. This gives the possibility to supply the chip core either with the battery or with the charger depending on the conditions. Bulk switch comparators are used to avoid any parasitic current flow. To ensure high PSRR and stability, a low-ESR ceramic capacitor of min. 1µF must be connected to the output.

Parameter

Figure 29:
Low power LDO (V2_5) Characteristics, V_{BAT}=3.7V; ILOAD_ext=0; Tamb=25°C; CLOAD =1µF (Ceramic); unless otherwise specified

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{BAT}	Supply voltage rage		2.7		5.5	V
V_{USB}			4.2		5.5	
R_{ON}	On resistance	Guaranteed per design		50		Ω
I_{OFF}	Shut down current			100		nA
I_{VDD}	Supply current	Guaranteed per design, consider chip internal load for measurements.		3		µA
I_{out}	Output current	Maximum external load			2	mA
t_{start}	Startup time			200		µs
V_{out}	Output voltage		2.4	2.5	2.6	V

DCDC Step-Up Converter

Description

The DC/DC Step Up converter is a high efficiency current mode PWM regulator, which provides an output voltage dependent on the maximum VDS voltage of the external transistor, and maximum load current selectable by the external shunt resistor.

For Example:

- 5V, 0.5-1A @ 1Mhz
- 25V, 50mA @ 1MHz
- 40V, 20mA @ 500kHz

A constant switching frequency results in a low noise on supply and output voltage. Step-up converter 1 is not available in CSP64 package.

Figure 30:
DC/DC step-up Converter 1

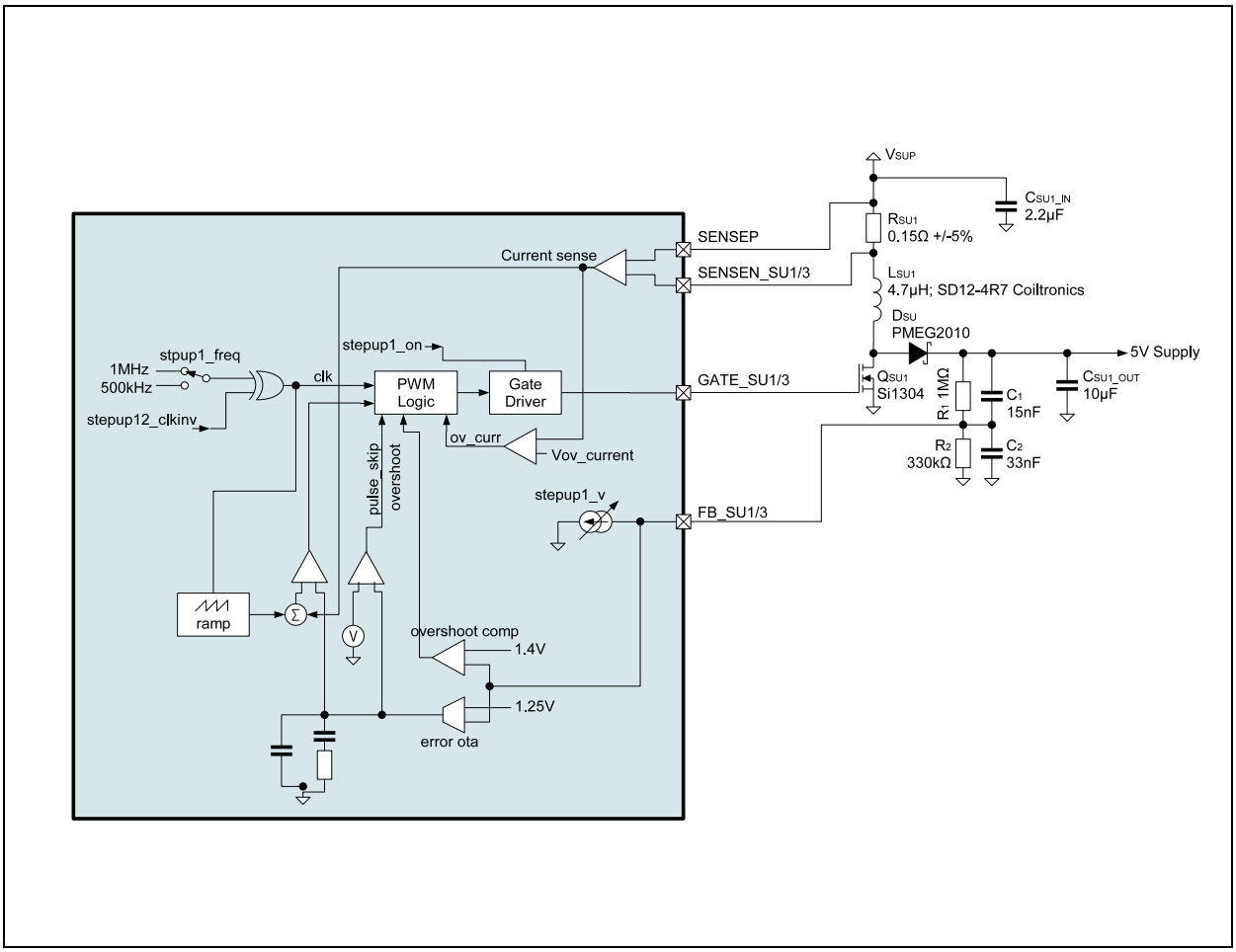
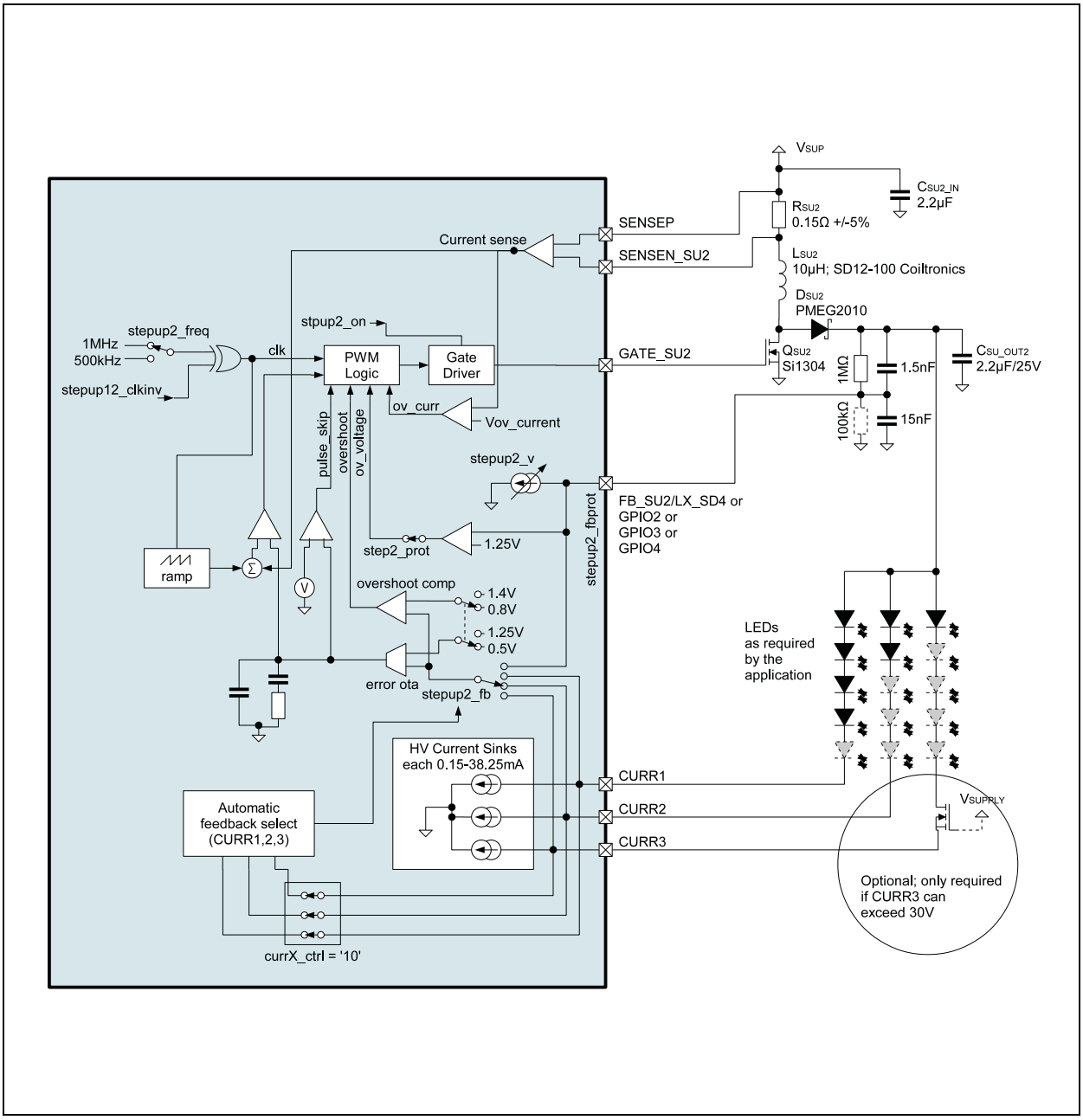


Figure 31:
DC/DC step-up Converter 2



Feedback selection SU1

For step up SU1, the feedback is always FB_SU1.

Feedback Selection SU2

For step up SU2 following feedback selections are possible (selected by setpup2_fb): (see Figure 31)

Current Feedback

CURR1, CURR2 or CURR3 can be selected by stepup2_fb as a current feedback pin.

The step-up converter is regulated such that the required current at the feedback path can be supported. stepup2_fbprot selects the overvoltage protection feedback pin (LX_SD4, GPIO2, GPIO3 or GPIO4). In this mode the output voltage will be limited by limiting the voltage on the selected feedback pin to 1.25V (select the external resistor network and stepup2_v to adjust this limitation voltage).

stepup2_prot_dis has to be set to 0, otherwise the protection is disabled.

Always choose the path with the higher voltage drop as feedback to guarantee adequate supply for the other, unregulated path.

Current Feedback with Automatic Feedback Selection

Same as above, but when currX_ctrl = 10b for the used current sinks, the chip automatically selects the highest string (CURR1, CURR2 or CURR3) as feedback input.

Voltage Feedback

stepup2_fb = 00b. LX_SD4, GPIO2, GPIO3 or GPIO4 can be selected by stepup2_fbprot as a voltage feedback input.

The step-up converter output voltage is regulated by regulating the selected feedback pin voltage to 1.25V.

Calculating Resistors for Voltage Feedback or Over-Voltage Protection

Bit stepupX_res should be set to 1 in voltage feedback mode using two resistors.

The output voltage is regulated to a constant value, given by:

(EQ1) $$V_{SU} = \frac{R_1 + R_2}{R_3} \times 1,25 + I_{FB} \times R_1$$

If R2 is not used, the output voltage is:

(EQ2) $$V_{SU} = 1,25 + I_{FB} \times R_1$$

V_{SU}: Step up regulator output voltage

R_1 : Feedback resistor R1

R_2 : Feedback resistor R2

I_{FB}: Tuning current on DCDC_FB pin: stepupX_v (0 to 31µA (1µA steps))

Example:

Figure 32:
Step Up Output Voltage (Voltage mode or protection voltage)

$I_{FB\ (stepupX\_v)}$	V_{SU}	V_{SU}
µA	R1=1MΩ, R2 not used	R1=500kΩ, R2=64kΩ
0	-	11
1	-	11.5
2	-	12
3	-	12.5
4	-	13
5	6.25	13.5
6	7.25	14
7	8.25	14.5
8	9.25	15
9	10.25	15.5
10	11.25	16
11	12.25	16.5
12	13.25	17
13	14.25	17.5
14	15.25	18
15	16.25	18.5

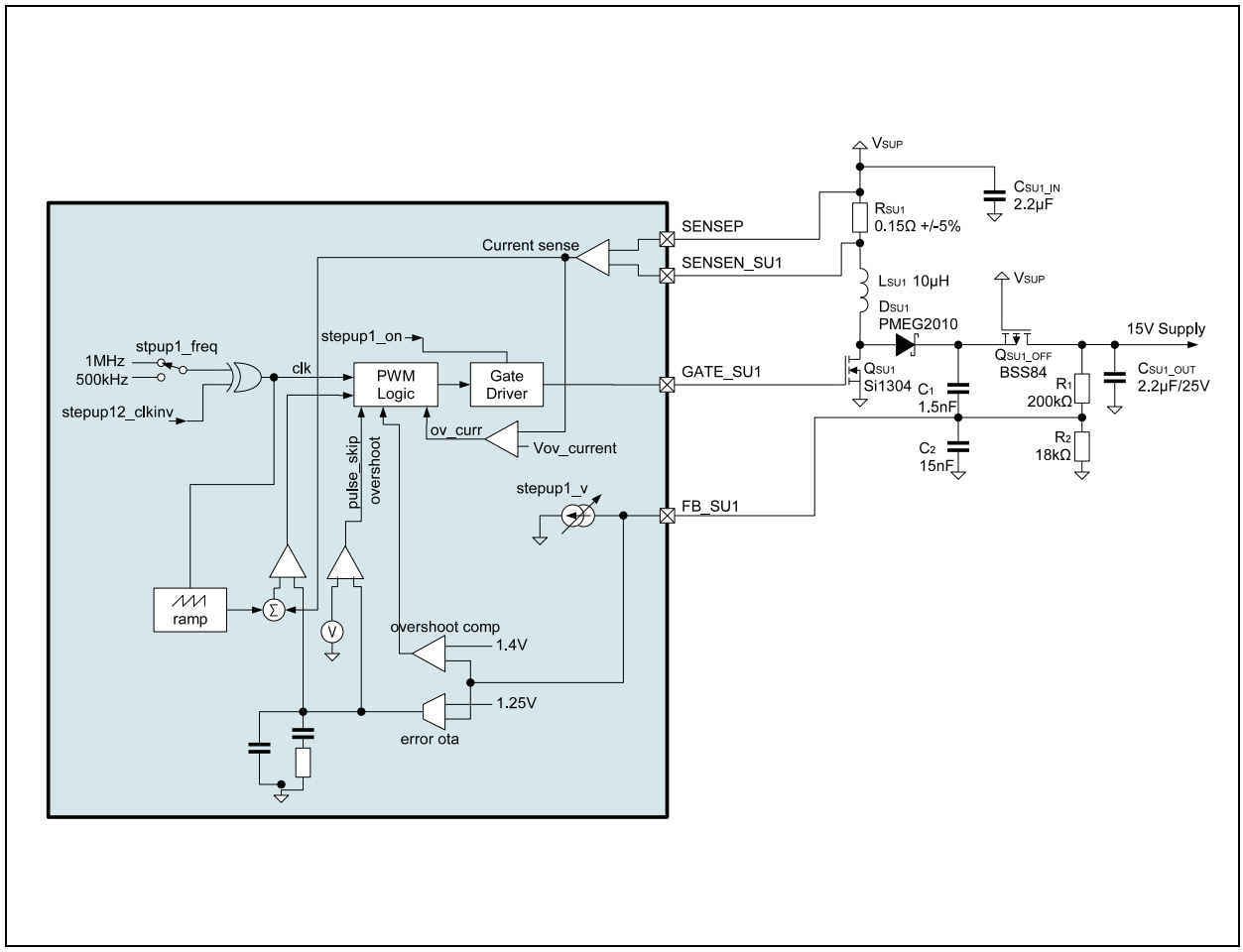
Note(s) and/or Footnote(s):
1. The voltage on pin CURR1, CURR2 and CURR3 must never exceed 30V.

Output Disconnect

As the output voltage is always ON, an additional output transistor can be added to reduce shutdown current through R1, R2 and the connected output circuit.

Note(s): A similar circuit can be used for step up converter 2.

Figure 33:
StepUp 1 with regulated output voltage (15V), and switch OFF function of output voltage, to reduce shutdown current

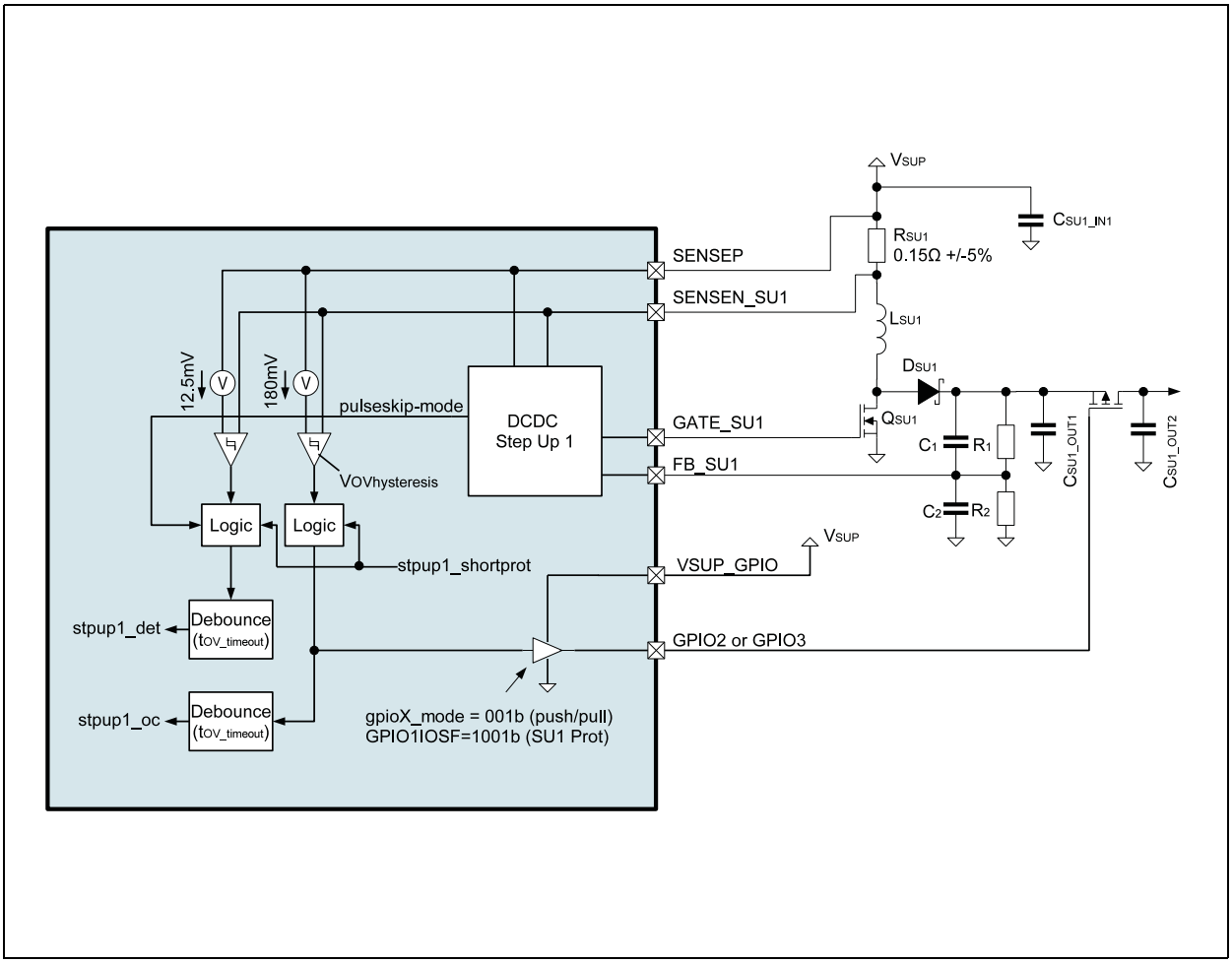


StepUp1 Load Detection and Over-current Protection Circuit

This circuit protects the DCDC step up1 converter during short circuit and startup, by regulation of the output current. An additional feature is the detection of a minimum output load of the Step-up converter. It is also possible to use this circuit without the DCDC step up converter, by using the sense resistor only:

- **Detection circuit:** If the voltage on R_{sense} exceeds V_{DETECT} for more than 1ms, or the DCDC Step up converter is not in pulse-skip for more than 1ms, the stepup1_det bit will be set.
- **Over-current protection:** If the Over-current voltage $V_{OVCURRENT}$ has been exceeded by more than 5ms the bit stpup1_oc will be set and can only reset, by switching OFF and ON the Protection circuit by writing stpup1_shortprot 0 – 1. If stpup1_oc is set the load will be disconnected, if stpup1_oc_timeout=1

Figure 34:
StepUp 1 Load Detection and Over-current Protection Application Circuit



Parameter

Figure 35:
DC/DC Step-up Controller Parameters

Symbol	Parameter	Note	Min	Typ	Max	Unit
I_{VDD}	Quiescent Current	Pulse skipping mode		140		µA
V_{FB1}	Feedback voltage for external resistor divider:	For constant voltage control	1.20	1.25	1.30	V
V_{CURR}	Feedback voltage for current sink regulation	CURR1, CURR2 or CURR3		0.6		V
I_{DCDC_FB}	Additional tuning current at FB_SUx	Adjustable by software in 1µA steps	0		31	µA
	Accuracy of feedback current	@ full scale	-7		7	%
V_{rsense_max}	Current limit voltage at Rsense	E.g.: 0.65A for 0.15Ω sense resistor		100		mV
R_{SW}	switch resistance	ON-resistance of external switching transistor			1	Ω
I_{load}	Load current	At 25V output voltage	0		50	mA
f_{IN}	Switching frequency	Internal CLK frequency/4, default 1MHz		f_{clk_int} /4		MHz
t_{MIN_ON}	Minimum ON time			130		ns
MDC	Maximum duty cycle	@ 1MHz		91		%

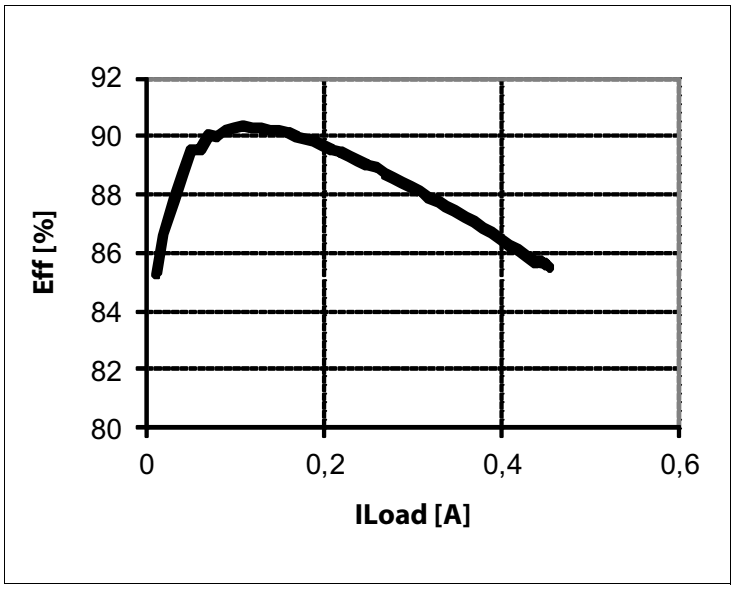
Figure 36:
StepUp1 Protection/Detection Circuit Parameters

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{DETECT}	Detection Threshold	For Rsense=0.150Ω => 83mA typ.	2	12.5	25	mV
$V_{OVCURRENT}$	Over-current Threshold rising	For Rsense=0.150Ω => 1.2A typ.	150	180	215	mV
$V_{OVhysteresis}$	Over-current Hysteresis			50		mV
$t_{OV\_timeout}$	Over-current timeout	Interrupt and/or external PMOS switching OFF after timeout f_{clk_int} = 2.2MHz		5		ms
t_{detect}	Detection de-bounce time	f_{clk_int} = 2.2MHz		1		ms

Figure 37:
DC/DC Step-up Controller External Components

Symbol	Parameter	Note	Min	Typ	Max	Unit
C_{out}	Output capacitor	Ceramic, ±20%		2.2		µF
L_{SU}	Inductor	Use inductors with small $C_{parasitic}$ (<100pF) to get high efficiency; Vout >8V		10		µH
		Use inductors with small $C_{parasitic}$ (<100pF) to get high efficiency; Vout <8V		4.7		µH
Q_{SU}	Transistor	$V_{GS(TH)}$ threshold voltage		1.3	1.5	V
		V_{DS} max drain to source voltage	V_{out_max} +20%			V
		$R_{DS(ON)}$ drain -source on resistance		0.35		Ω
		Q_{GS} total gate charge @ V_{GS}=4.5V		3	5	nC
C_1 / C_2	Feedback capacitor ratio	Ratio should be smaller than the feedback resistor ratio (inverted) to avoid overshoots during start-up			R2/R1	µF

Figure 38:
Step-Up DC/DC Controller Efficiency vs. Output Current; V_{SUP} = 3.8V, T_A = +25°C



Current Sinks

Description

These are general-purpose current sinks intended to control the backlight(s), buzzer and vibrator.
CURR1 and CURR2, CURR3 are high voltage (30V) current sinks, e.g. for series of white LEDs. CURR2 is not available in CSP package.

Current sinks CURR1, CURR2 and CURR3 can be controlled individually. The step-up DCDC converter (SU2) may supply them with voltages up to 30V. For an automatic feedback selection the used current sinks can be assigned to the SU2 booster.

If not used as a current sink, CURR3 can be used to output several status signals. In this mode the CURR3 output acts like an open-drain output and needs an external pull-up resistor for generating logic high levels.

Parameter

Figure 39:
Current Sinks Characteristics

Symbol	Parameter	Note	Min	Typ	Max	Unit
$I_{CURR1,2,3}$	CURR1,2 & 3 current, 00h-3Fh	For V(CURRx) > 0.5V resolution = 0.1563mA	0		39.84	mA
$I_{DCDC\_protect}$	Current sink protection Current	Protection Current if stpup2_on=1 and currx_current=00h		2		µA
Δ	Absolute Accuracy	All Current sinks	-8		+8	%
$V_{CURR1,2,3}$	Voltage compliance	During normal operation	0.5		30	V

Charger

Description

The AS3711 device serves as a standalone battery charge controller supporting rechargeable lithium Ion (Li+) batteries. Requiring only a few external components, a full-featured battery charger with a high degree of flexibility can easily be realized. The main features of the controller are:

- Charge adapter detection
- PowerPath management & internal voltage regulator (V2_5), for dead battery startup
- Low current (soft) charging
- Low current (trickle) charging
- Constant current charging
- Constant voltage charging
- 30V Overvoltage protection
- Battery presence indication
- Operation without battery
- Input current limitation
- Input voltage drop regulation
- Programmable linear or switched mode operation
- Bypass mode for high input current application (up to 6A)

Figure 40:
Charger Application Block Diagram, Step Down Charger Mode

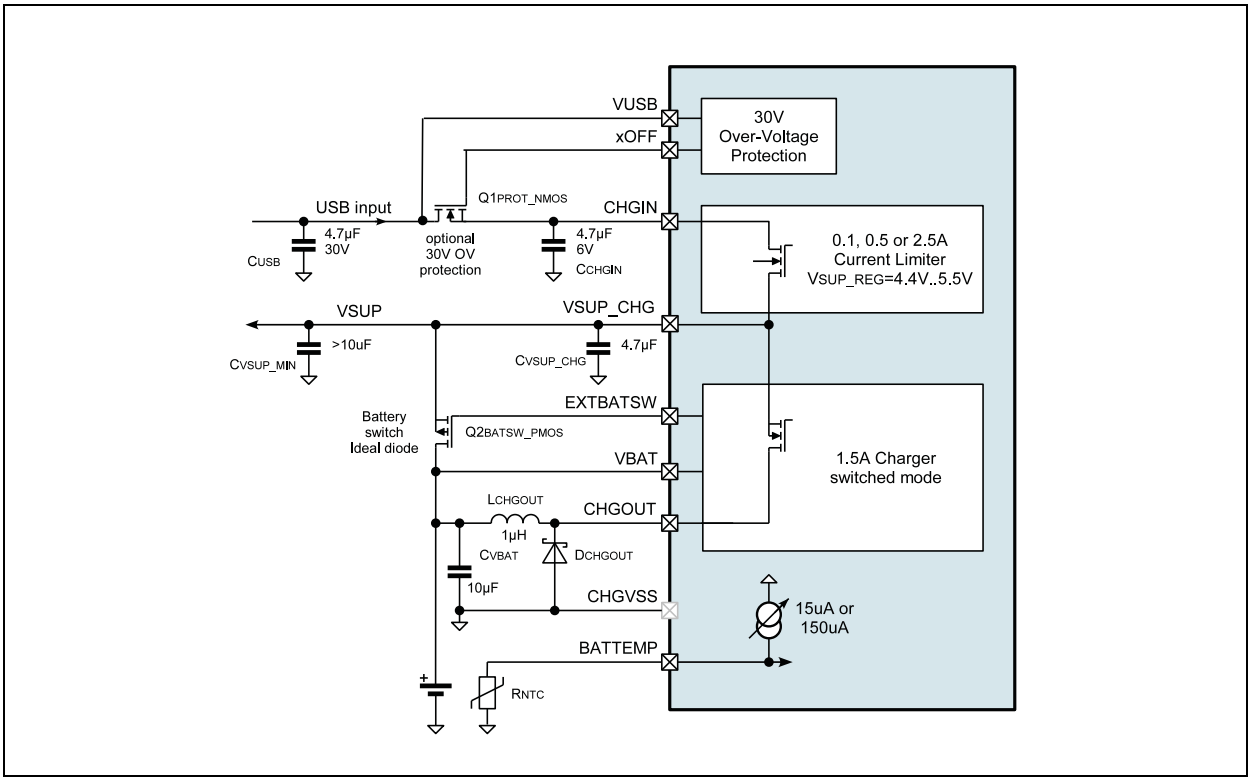
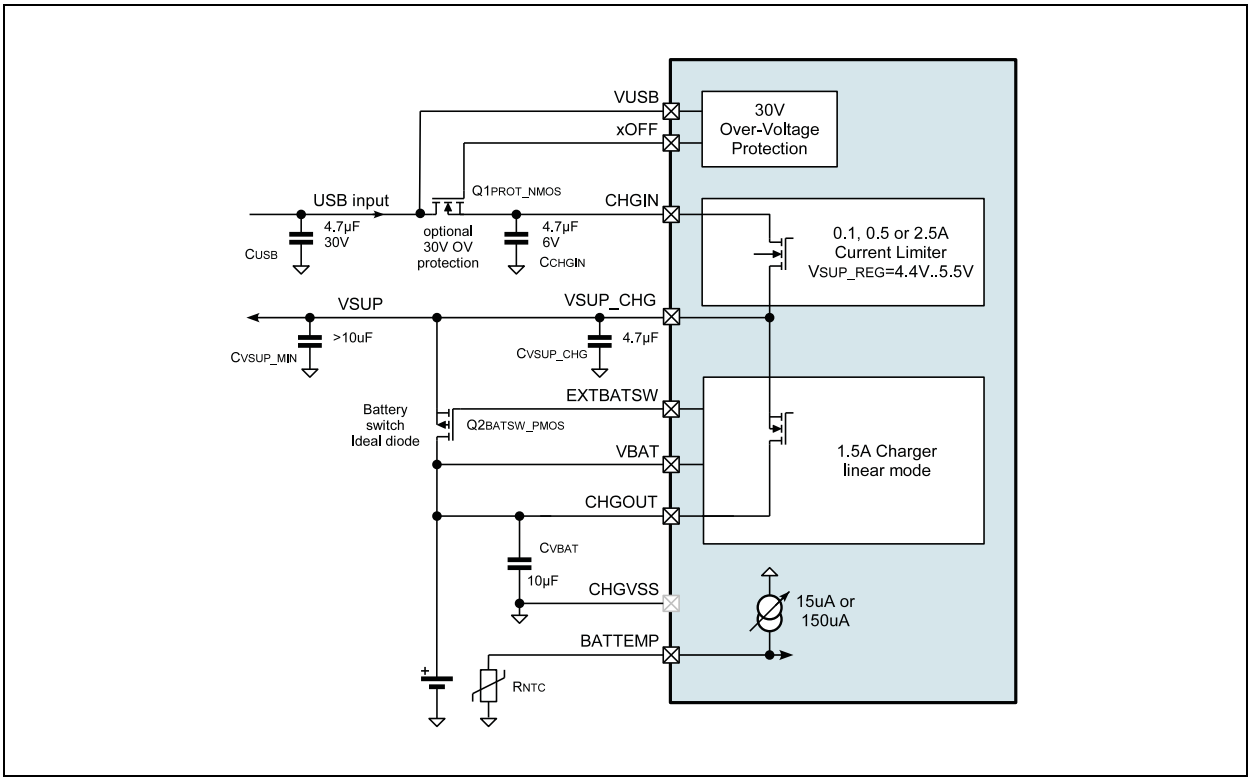


Figure 41:
Charger Application Block Diagram, Linear Charger Mode



Charging Cycle Description

Charge adapter detection

The charge controller uses an integrated detection circuit to determine if an external charge adapter has been applied to the VUSB pin. If the adapter voltage exceeds the battery voltage at pin VBAT by V_{CHDET} the *ChDet* bit in the *ChargerStatus* register will be set. The detection circuit will reset the charge controller (bit ChDet is cleared) as soon as the voltage at the VUSB pin drops to only V_{CHMIN} above the battery voltage. In case the AS3710AS3711 device is reset the charge controller will also be reset, even if a charge adapter is applied to the VUSB pin.

Soft charging

Soft charge mode is started when an external charge adapter has been detected, the bat_charging_enable is set and the battery voltage at pin VBAT is below the V_{SOFT} threshold.

Low current (trickle) charging

Trickle charge mode is started when an external charge adapter has been detected *bat_charging_enable* is set and the battery voltage at pin VBAT is below the $V_{TRICKLE}$ threshold and above VSOFT threshold; bits ChDet and Trickle will be set in the *ChargerStatus* register. In this mode the charge current will be limited to TrickleCurrent (set in the *ChargerCurrent* register) to

prevent undue stress in case of deeply discharged batteries. Once $V_{TRICKLE}$ has been exceeded, the charger will change over to constant current charging (Trickle is cleared).

Constant current charging

Constant current charging is initiated when *bat_charging_enable* is set and the battery voltage at pin VBAT is above the $V_{TRICKLE}$ and below V_{CHOFF}. The CCM bit is set when the charger has started, and the charge current will be limited to ConstantCurrent by the battery charge controller. When the battery approaches full charge, its voltage will reach the charge termination threshold V_{CHOFF}. V_{CHOFF} depends on the ChVoltEOC bits settings. Top-off charge will be started (CVM will be set).

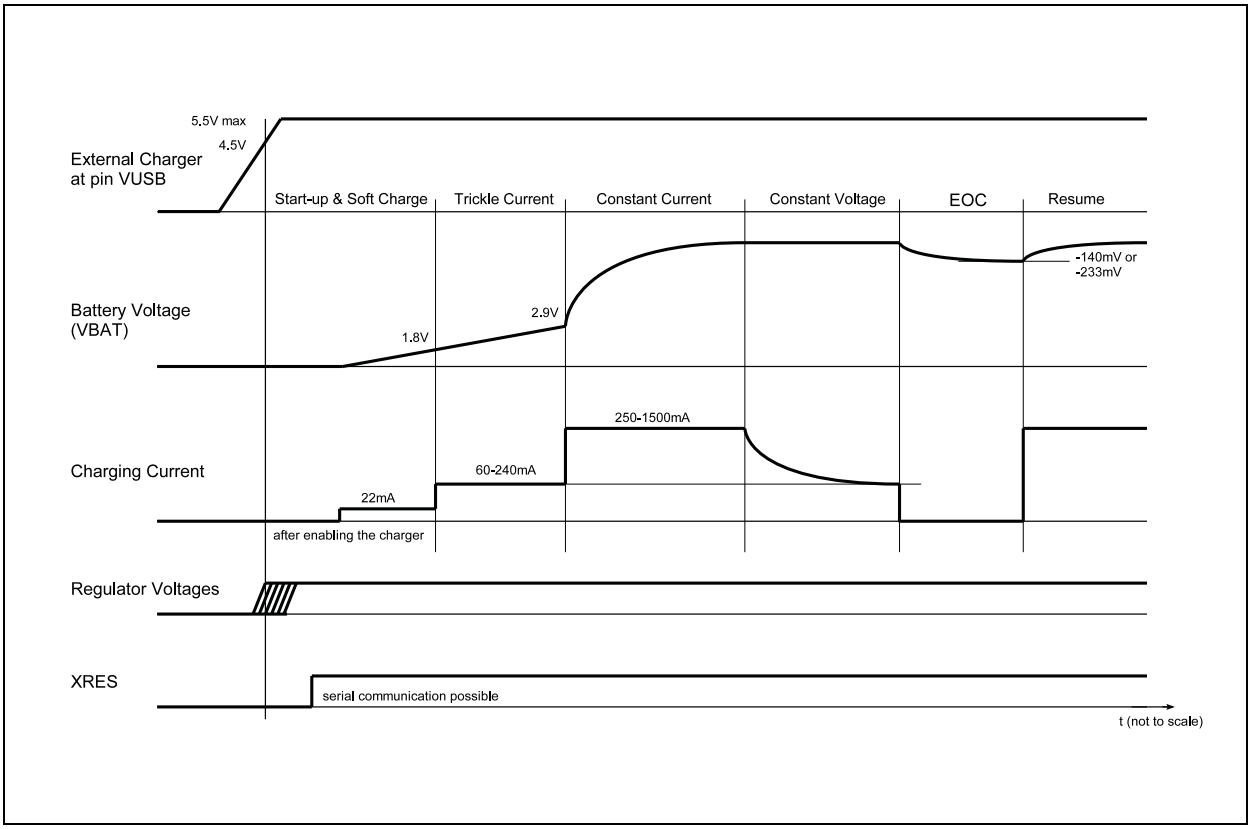
Constant voltage charging

Constant voltage charge mode is initiated and the CVM bit will be set when the V_{CHOFF} threshold has been reached.

The charge current is monitored during constant voltage charging. It will be decreasing from its initial value during constant current charging and eventually drop below the value set by TrickleCurrent. If the measured charge current is less than or equal to TrickleCurrent, the charging cycle is terminated and EOC is set.

Charger States

Figure 42:
Charger States Diagram



Stop charging conditions

There are multiple safety features implemented that trigger a stop_charging condition:

These are the following:

- Battery temperature too high. If *ntc_on*=1 and voltage at pin NTC is below $V_{BATTEMP}$
- Timeout timer expired (If *ch_timeout*>0 and charging time has been exceeded. (Can be reset by unplugging the charger, setting *chg_on*=0 or writing *charging_tmax*=0)
- VUSB over-voltage detected
- Die temp>140deg (ov_temp_140 set)

Battery presence indication and operation without battery

After EOC state is reached a timer for NOBAT detection is started. If there is no battery present, the VBAT voltage will drop to V_{RESUME}. Depending on the load on VBAT and the capacitor on VBAT this might take some milliseconds to 1 second. If the RESUME mode is enabled (Bit auto_resume=1), the charger will restart charging (ConstantCurrent charging) after 100msec delay.

The 100msec dead time is necessary to get a battery oscillation frequency below 10Hz, if there is no battery present.

If the NOBAT detection timer is below 2 seconds after reaching EOC state, and this happens 2 times in serial, the Nobat bit in ChargerStatus register is set. If an battery is inserted the bit will be reset after the timer exceeds the 2 seconds.

In addition, if the nobat_ntc_det bit is set the looping will be stopped and a NTC detection is started.

A pull up current of 0.5uA is applied to BATTEMP. If the BATTEMP voltage is above 1.8V, the state machine stays in the no bat state. If the BATTEMP voltage is below 1.8V, a charging cycle is initiated.

Charger overvoltage protection

This blocks checks if the charger voltage VUSB is above V_{CHOVH}. If the VUSB voltage is above VCHOVH , the pin XOFF is pulled to GND immediately, to protect the pin VCHG_IN, and the charger is set into OFF state. If the VUSB voltage is below V_{CHOVH} the XOFF pin is charged up to V_{XOFF_REG} with an integrated charge pump. If the pin exceeds V_{XOFF_MIN} the usb_prot_ready bit is set and the charger is started.

NTC supervision

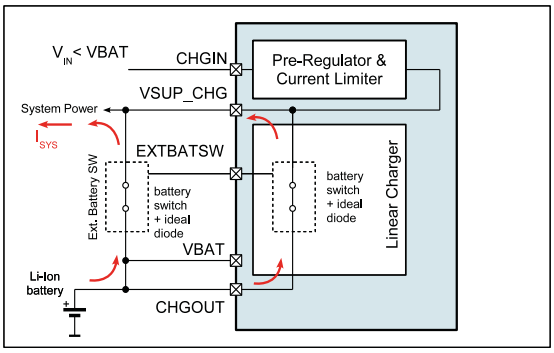
This charger block also features a supply for an external NTC resistor to measure the battery temperature while charging. If the temperature is too high (voltage on BATTEMP pin is below VBATTEMP_ON) the charger will stop operation. If needed an interrupt can be generated based on this event. When the battery temperature drops the voltage on BATTEMP pin will rise above VBATTEMP_OFF and the charger will start charging again. This is forming a temperature hysteresis of about 3 to 5°C to avoid an oscillation of the charger.

The levels for switching OFF the charger (ntc_temp: 45°C or 55°C) as well as the type of NTC (ntc_10k: 10k or 100k) can be selected via register settings. The battery temperature supervision via the NTC can be switched OFF (ntc_on = 0).

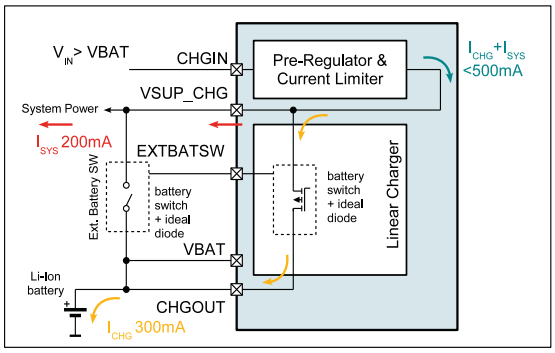
The supply for the NTC will be only on when a charger is detected and ntc_on bit is set.

Charger Modes

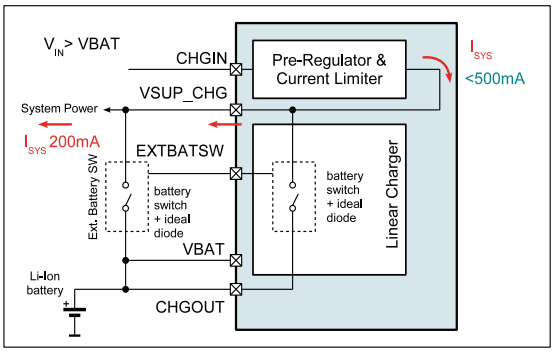
Figure 43:
Linear Charger Modes



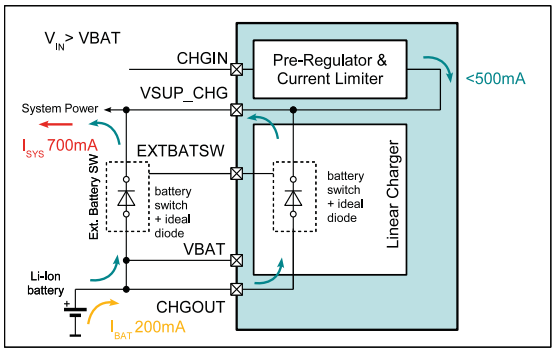
In normal operation, when the charger is not connected, all the system current comes out of the battery



During charging the charger is active. The system and the charger are supplied from the pre-regulator output.
If (I_{SYS} + I_{CHG}) exceed the chosen current limit, I_{CHG} will be reduced automatically (VSUP_x gets lower than VSUP_MIN).

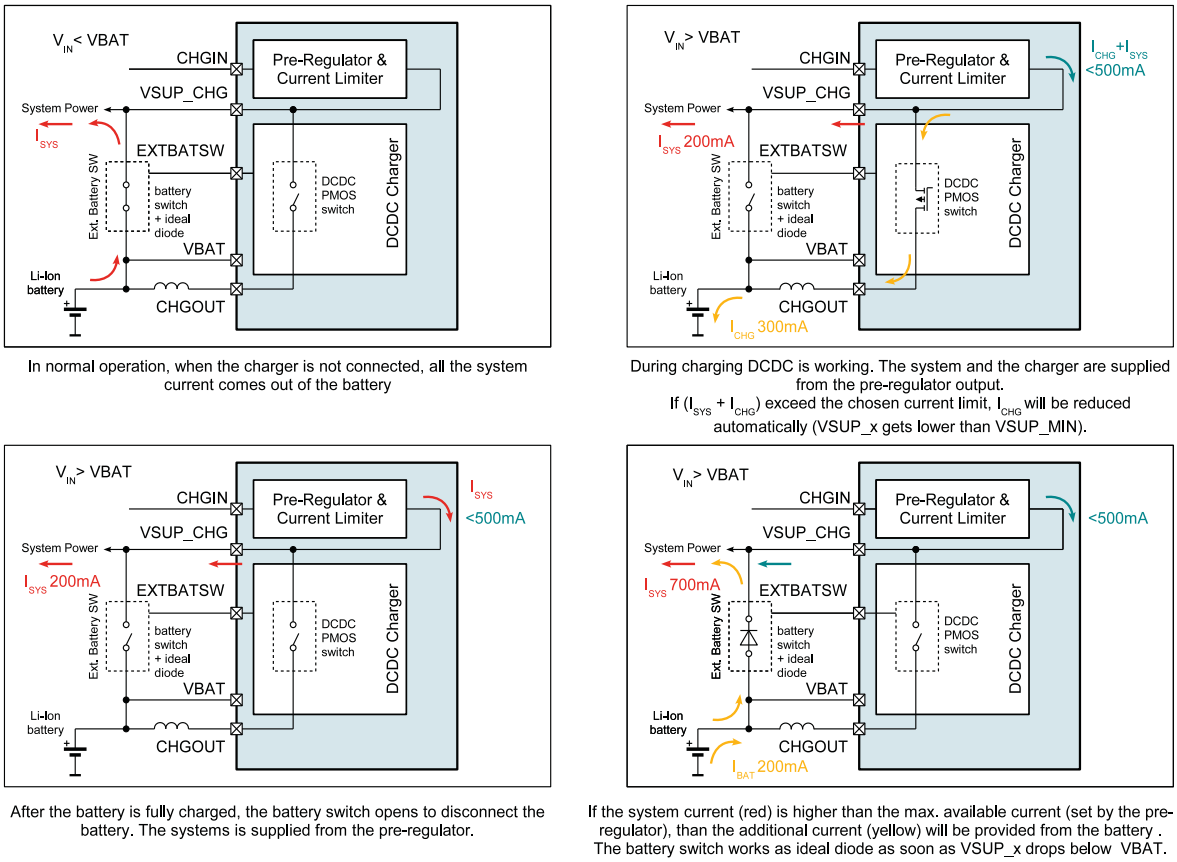


After the battery is fully charged, the battery switch opens to disconnect the battery. The systems is supplied from the pre-regulator.



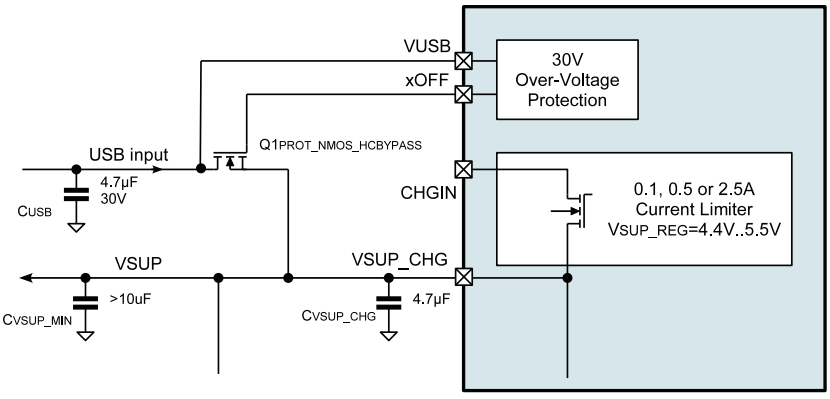
If the system current (red) is higher than the max. available current (set by the pre-regulator), than the additional current (yellow) will be provided from the battery . The battery switch works as ideal diode as soon as VSUP_x drops below VBAT.

Figure 44:
DCDC Charger Modes



Alternative Charger Input Configurations

Figure 45:
Charger with Current Limiter Bypass



Parameter

T_A= 25°C, unless otherwise specified.

Figure 46:
Charger Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CHDET}	Charger Detection threshold	VUSB-VBAT Hysteresis is > 40mV	50	75	105	mV
V_{CHMIN}			0	20	35	mV
V_{SOFT}	Apply ISOFT charging current below that VBAT voltage			1.8		V
I_{SOFT}	Charging current if VBAT is below VSOFT			22		mA
$V_{TRICKLE}$	Trickle to CC current threshold	V_{BAT} rising		2.9		V
$I_{TRICKLE}$	Trickle/EOC current limit	Programmable in 60mA steps		60.. 240		mA
V_{CHOFF}	Charge termination threshold	Programmable in 20mV steps between 3.5 and 4.44V		3.5.. 4.44		V
		@ ChVoltEOC=35 (4.2V)	4.15	4.20	4.242	V
I_{CC}	CC current limit	Programmable in 50mA steps		250.. 1500		mA
		Linear charging mode	-10%		+10%	mA
I_{USB_limit}	USB input current limit	@ 470mA	-7%	470	+6%	mA
VRESUME	Resume voltage limit to start charger	VBAT falling threshold (depending on ChVoltResume)		140/ 233		mV
VSUP_min	VSUP level for charging current regulation (reduction), to avoid voltage drop on VSUP	Trickle current (or constant current in linear mode) will be regulated down, if VSUP drops below this level	-6%	3.9	3%	V
				4.2		
				4.5		
				4.7		
IREV_OFF	Reverse current shut down	VSUP_CHG = 5V, VUSB open		5		µA
V_{Diode}	Ideal Diode start voltage			50		mV
R_{ON_BATSW}	Battery Switch ON-resistance			0.10		Ω

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Temp Supervision						
$V_{BATTEMP\_ON}$	Battery Temp. high level (50 or 55°C)	VSUP >3V NTC_{beta}=4200		500 or 400		mV
$V_{BATTEMP\_OFF}$	Battery Temp. low level (45 or 50°C)	VSUP >3V NTC_{beta}=4200		600 or 500		mV
$I_{BATTEMP}$	NTC Bias Current	100kΩ NTC 10kΩ NTC	-15%	15 150	+15%	µA
XOFF overvoltage protection						
V_{CHOVH}	VUSB Overvoltage Detection	Monitor voltage on VUSB, disable charging beyond this voltage (200mV hysteresis)		6.2	+3%	V
			-3%	6.0		
V_{XOFF_min}	Minimum XOFF voltage for charger startup			7.5		V
V_{XOFF_REG}	Regulation voltage for XOFF pin			10		V
I_{XOFF}	External pull down current on XOFF pin	Connect XOFF pin to MOSFET gates only			100	nA

Figure 47:
External Components

Symbol	Parameter	Note	Min	Typ	Max	Unit
$Q1_{PROT\_NMOS}$	FDN337N	Vds=30V, 2.2A		65		mΩ
	FDN339AN	Vds=20V, 3A		35		mΩ
	FDN327N	Vds=20V, 2A		70		mΩ
	FDG311N	Vds=20V, 1.9A		115		mΩ
	Si1472DH			82		mΩ
$Q1_{PROT\_NMOS\_HC\ BYPASS}$	FDC637AN	Vds=20V, 6.2A		24		mΩ
	FDT439N	Vds=30V, 6.3A		45		mΩ
$Q2_{BATSW\_NMOS}$	FDN306P	@ 4.5V		40		mΩ
	FDC602	@ 4.5V		33		mΩ
	FDC642	@ 4.5V		65		mΩ
C_{USB}	Bypass capacitor on VUSB pin	±20%, X5R or X7R dielectric / 25V		4.7		µF

Symbol	Parameter	Note	Min	Typ	Max	Unit
C_{VSUP_CHG}	Bypass capacitor on VSUP_CHG	X5R or X7R dielectric near to pin VSUP_CHG		4.7		µF
C_{VSUP_MIN}	Bypass capacitor on VSUP	X5R or X7R dielectric, total value	10			µF
C_{VBAT}	Bypass capacitor on VBAT	X5R or X7R dielectric		10		µF
L_{CHGOUT}	LQM2HPN1R0MJ0 (MURATA)	Ron=90mOhm / 1.5A rated current		1		µH
	MLP2520S1R0M (TDK)	Ron=85mOhm / 1.5A rated current		1		µH
D_{CHGOUT}	PMEG2010 (NXP)			1		A
	NSR10F20NXT5G (ONSEMI)			1		A

Figure 48:
Step-Down vs Linear Charger; V_{SUP} = 4.5/5.0V, T_A = +25°C

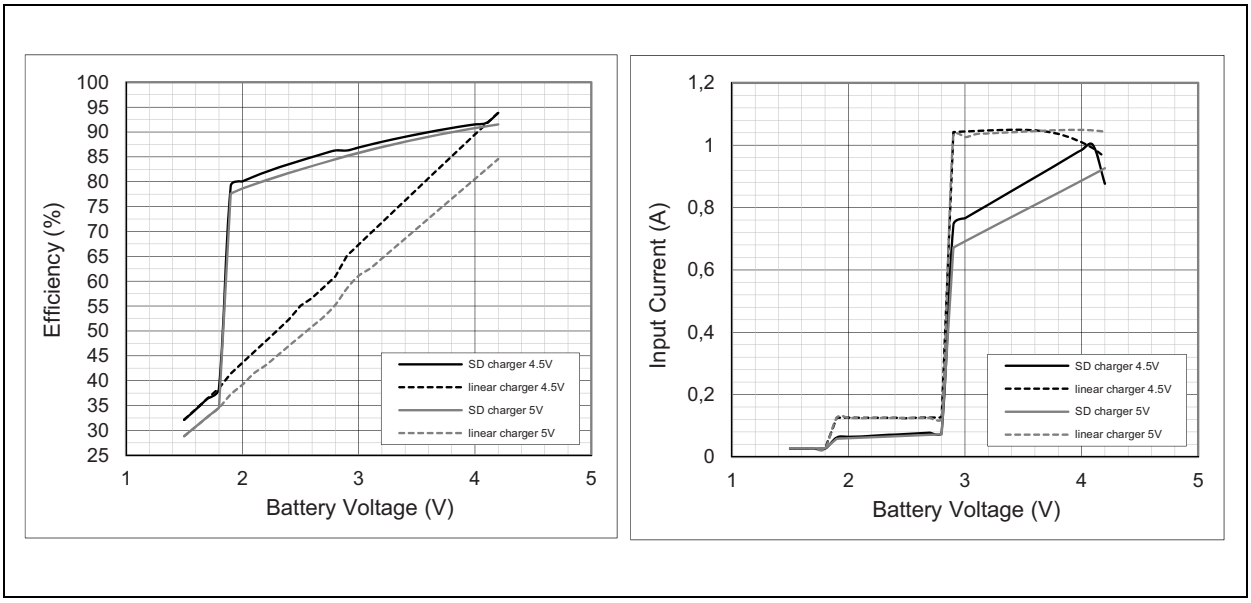
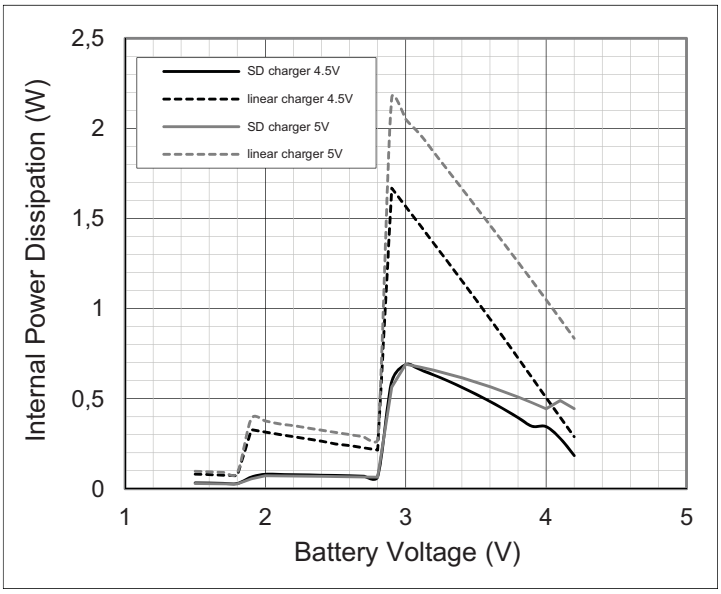


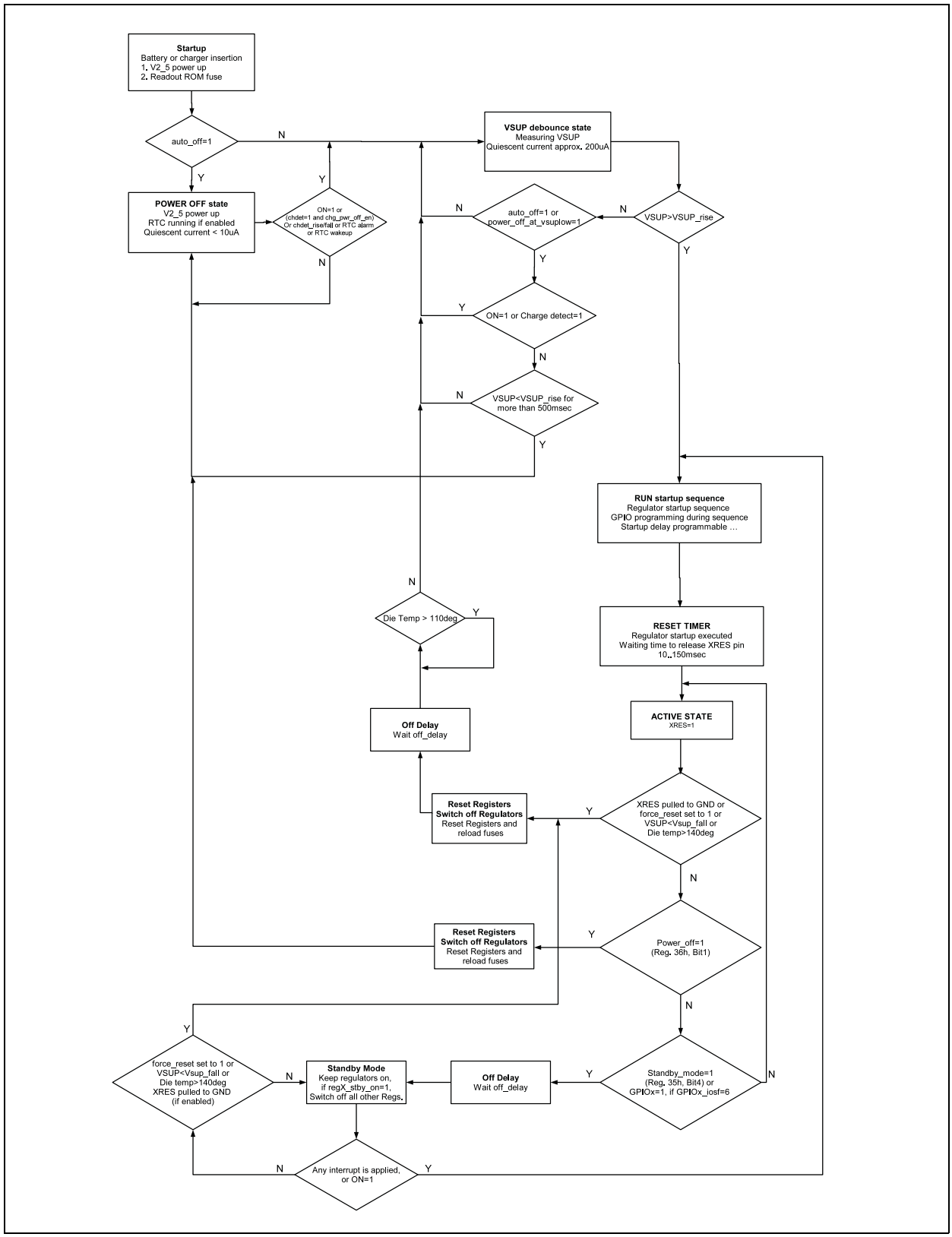
Figure 49:
Step-Down vs Linear Charger; V_{SUP} = 4.5/5.0V, T_A = +25°C



Detailed Description - System Functions

Start-up

Figure 50:
Startup Flow Chart



Normal Startup

During a normal reset cycle (e.g. after the battery or a charger is inserted), after V2_5 is above V_{POR} and VSUP is above ResVoltRise a normal startup happens:

- The external capacitor on CREF is charged to 1.8V.
- Configuration of Charger (DCDC or linear) and SD2/SD3 (combined mode or separated) is read from the Boot-OTP.
- Startup State machine reads out the internal Boot-OTP. The start-up sequence of Step-Down Converter, LDO's and GPIOs are controlled by the Boot-OTP.
- Reset-Timer is set by the Boot-OTP
- The reset is released when the Reset Timer expires (external pin XRES)

Startup from Charger

If the voltage on pin VUSB is within $VSTART_{CHARGER}$, the AS3711 is started (even with V_{BAT} = 0V). This allows the battery to be charged (even from deeply discharged batteries) and finally a normal startup to happen.

Parameter

Figure 51:
Charger and ON-input Startup Conditions

Symbol	Parameter	Note	Min	Typ	Max	Unit
$VSTART_{CHARGER}$	Voltage on VUSB for system to start	on Pin VUSB	4.2	5.0	30	V
V_{ON_IL}	ON Low Level input voltage		–0.3		0.4	V
V_{ON_IH}	ON High Level input		1.4		V_{VSUP_GPIO}	V
I_{ON_PD}	ON Pull down current		4	12		µA

Reset

Description

XRES is a low active bi-directional pin. An external pull-up to the periphery supply has to be added.

During each reset cycle the following states are controlled by the AS3711:

- Pin XRES is forced to GND
- Normal startup with programmable power ON sequence and regulator voltages (see Start-up on page 52)
- Reset is active until the programmable reset timer (set by register bits *res_timer*<2:0>) expires
- All registers are set to their default values after power ON, except the reset control- and status-registers.
- XRES is pulled high by the external resistor and the whole system is leaving the reset state

Note(s): Programming is controlled by the internal Boot-OTP.

Parameter

Figure 52:
XRES-input Characteristics

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{XRES_IL}	XRES Low Level input voltage		-0.3		0.4	V
V_{XRES_IH}	XRES High Level input voltage		1.4		VSUP_GPIO	V

Reset Conditions

Reset can be activated from 7 different sources:

- Power ON (battery or charger insertion)
- Low Battery
- Software forced reset
- Power OFF mode
- External triggered through the pin XRES
- Over-temperature
- Watchdog
- On-key long press

Voltage Detection:

There are two types of voltage dependent resets: V_{POR} and V_{XRES}. V_{POR} monitors the voltage on V2_5 and V_{XRES} monitors the voltage on VSUP. The linear regulator for V2_5 is always ON and uses the voltage CHGIN or VBAT VSUP as its source.

The pin XRES is only released if V2_5 is above V_{POR} and VSUP is above ResVotlRise.

Figure 53:
Reset Levels

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{POR}	Overall power ON reset	Monitor voltage on V2_5; power ON reset for all internal functions	1.5	2.0	2.3	V
$VRES_{RISE}$	Reset level for Vsupply rising	Monitor voltage on VSUP; rising level		ResVolt Rise (1)		V
$VRES_{FALLING}$	Reset level for Vsupply falling	Monitor voltage on VSUP; falling level		2.7		V
		If SupResEn=1 only		ResVolt Fall		V
$VRES_{MASK}$	Mask time for $VRES_{FALLING}$. Duration for V_{BAT}<ResVoltFall until a reset cycle is started (2)	FastResEn = 0		3		ms
		FastResEn = 1		4		us

Note(s) and/or Footnote(s):

1. It's recommended to set the ResVoltRise level 200mV above the ResVolt Fall level to have a hysteresis.
2. XRES signal is de-bounced with the specified mask time for rising- and falling slope of V_{BAT}.
3. $VRES_{FALLING}$ is only accepted if the reset condition is longer than $VRES_{MASK}$. This guard time is used to avoid a complete reset of the system in case of short drops of V_{BAT}.

Power OFF:

To put the chip into ultra low power mode, write '1' into *power_off*. The chip stays in power OFF mode until the external pin ON is pulled high, the charger is inserted or the level V_{POR} is touched to start a complete reset cycle. The bit *power_off* is automatically cleared by this reset cycle. During *power_off* state all circuits are shut-off except the Low Power LDO (V2_5). Thus the current consumption of AS3711 is reduced to less than 15µA. The digital part is supplied by V2_5, all other circuits are turned OFF in this mode, including references and oscillator. Except the reset control registers all other registers are set to their default value after power ON.

Software forced reset

Writing '1' into the register bit *force_reset* immediately starts a reset cycle. The bit *force_reset* is automatically cleared by this reset.

External triggered reset:

If the pin XRES is pulled from high to low by an external source (e.g. microprocessor or button) a reset cycle is started as well.

Over-temperature reset:

The reset cycle can be started by over-temperature conditions. (see Supervisor on page 63)

Watchdog reset:

If the watchdog is armed (register bit wtdg_on = 1 and wtdg_res_on = 1) and the timer expires it causes a reset. (see Watchdog on page 64).

Long ON-key press:

When applying a high level on the ON input pin for 4s/8s (depending on on_reset_delay) a reset is initiated. This is thought as a safety feature when the SW hangs up and no watchdog is used.

Stand-by

Description

Stand-by allows shutting down a part or the complete system. Stand-by can be terminated by every possible interrupt or GPIO of the PMU. The interrupt has to be enabled and GPIO has to be configured before going to hibernation.

Figure 54:
Hibernation

State	Description
Enter via GPIO	To enter stand-by mode the following settings have to be done: • Enable just these IRQ sources which should lead to leave hibernation mode. • Make sure that IRQ is inactive (IRQ flags get cleared by register reading) • Set the GPIO to input (gpioX_mode = 0) -Set the GPIO for stand-by control (gpioX_iosf = 6) • Set regX_select and regX_voltage if another voltage is needed during stand-by for up to 3 regulators • Define which regulators should be kept powered during stand-by (sdX_stby_on, ldoX_stby_on) • Set chg_pwr_off_en to 1 • Activate the selected GPIO (going HIGH)
Enter via SW	To enter stand-by mode the following settings have to be done: • Enable just these IRQ sources which should lead to leave hibernation mode. • Make sure that IRQ is inactive (IRQ flags get cleared by register reading) • Set the delay for going into stand-by after the SW command (off_delay) • Define which regulators should be kept powered during stand-by (sdX_stby_on, ldoX_stby_on) • Set chg_pwr_off_en to 1 • Set standby_mode_on to 1
Hibernation	V2_5 chip supply is kept ON All other regulators are switched OFF dependent on the stby_on bits XRES goes active (can be disabled in the boot ROM) and pwr_good goes inactive
Leave	The chip will come out of stand-by with • IRQ activation or • ON key Start-Up sequence is provided defined by the boot ROM.

Internal References

The internal reference circuits needs the following external components:

Figure 55:
Reference External Components

Symbol	Parameter	Note	Min	Typ	Max	Unit
C_{EXT}	External filter capacitor	Ceramic low-ESR capacitor between CREF and VSS	-10%	100	+10%	nF

Low Power Mode

Use bit ***low_power_on*** to activate the Low Power Mode. In this mode the on-chip voltage reference and the temperature supervision comparators are operating in pulsed mode. This reduces the quiescent current of the AS3711 by 45uA (typ.). Because of the pulsed function some specifications are not fulfilled in this mode (e.g. increased noise), but still the full functionality is available.

Note(s): Low power mode can be controlled by the serial interface.

Parameter

Figure 56:
References Parameters

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{CEXT}	Reference Voltage	Low noise trimmed voltage reference – connected to Pad CREF; **do not load**	-1%	1.8	+1%	V
f_{CLK}	Accuracy of Internal reference clock	Adjustable by serial interface register clk_int	-12	f_{CLK}	+12	%

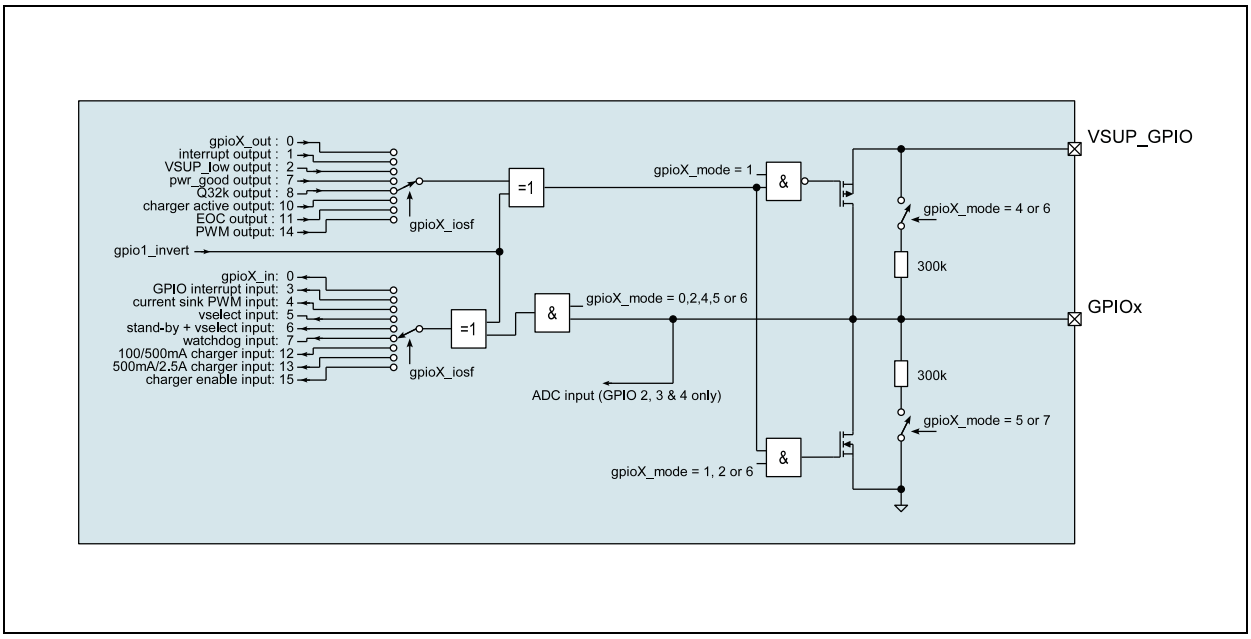
GPIO Pins

Description

The device contains 4 GPIO pins. Each of the pins can be configured as digital input, digital input (with pull-up or pull-down), ADC input (tri-state, or with pull down) only for GPIO2,3 and 4, push-pull output, or open drain output (with or without pull-up). When configured as output the output source can be a register bit, or the PWM generator.

The polarity of the input and output signals can be inverted with the corresponding gpioX_invert bit, all further descriptions refer to normal (noninverted) mode.

Figure 57:
GPIO Block Diagram



IO Functions

Normal IO operation:

If set to input, the logic level of the signal present at the GPIOx pin can be read from gpioX_in. If the output mode is chosen, gpioX_out specifies the logic level of the GPIOx pin.

This mode is also used for the ON/OFF controll of the DCDC and LDOs. The selection which regulator is controlled by which GPIO is done with the gpio_ctrl_sdX or gpio_ctrl_ldoX bits.

The gpioX_mode should be set to input.

Interrupt output:

GPIOx pin logic state is derived from the interrupt signal INT. Whenever an interrupt is present the GPIOx pin will be pulled high. The gpioX_mode should be set to output.

VSUP_low output

GPIOx pin will go high if VSUP falls below ResVoltFall and SupResEn = 0. The gpioX_mode should be set to output.

GPIO interrupt input

A falling or rising edge will set the gpio_int bit. The gpioX_mode should be set to input.

Current sink PWM input

The GPIO is used as PWM input for the current sink to control the current. 100% PMW mode will set the current to the value set by currX_current. The PWM control has to be enabled with currX_ctrl = 11b for each current sink to be controlled. The gpioX_mode should be set to input.

Vselect input

As long as the GPIOx pin is low the DCDC/LDOs operate with the normal register settings. If the GPIOx pin goes high the settings will change to the ones stored in regX_voltage. The gpioX_mode should be set to input.

The regulator affected by this mode is selected by regX_select. While GPIO3 & GPIO4 always control all regulators selected by regX_select, GPIO1 and GPIO2 may be used to control two regulators separately.:

Figure 58:
GPIO Vselect Modes

gpio1_iosf =	gpio2_iosf =	Vselect mode
<> 5	<> 5	No voltage select by GPIO for regulator
<> 5	5	GPIO2 controls regulator selected by reg1_select, reg2_select and reg3_select
5	<> 5	GPIO1 controls regulator selected by reg1_select, reg2_select and reg3_select
5	5	GPIO1 controls regulator selected by reg1_select GPIO2 controls regulator selected by reg2_select

Stand-by and Vselect input

This mode is very similar to the Vselct mode described in the previous paragraph. In addition to switch between 2 register settings of 3 regulators the chip is set into stand-by mode when the GPIOx pin goes high and wakes up again when the pin is pulled low and the gpio_restart_int is activated. The gpioX_mode should be set to input.

Only one GPIO is needed to control the stand-by function and voltage setting of all 3 selectable regulators. It's not recommended to set this mode (gpioX_iosf=6) for more than one GPIO at the same time. It's not possible to control the regulators by different GPIOs.

PWRGOOD output

This signal will go high at the end of the start-up sequence. This can be used as an second reset signal to the processor to e.g. start oscillators.
The gpioX_mode should be set to output.

Q32k output

When selected the GPIOx will provide the 32kHz RTC crystal frequency. If the oscillator is not enabled or not assembled the internal RC oscillator based clock will be used for the output. The gpioX_mode should be set to output.

Watchdog input

When pulling the GPIO high the watchdog will be triggered to avoid a reset cycle initiated by the watchdog. The gpioX_mode should be set to input.

SU1 OC output

This output signal can be used to control an external disconnect transistor if SU1 detects an over current condition. The gpioX_mode should be set to output.

Charger active output

When selected, the GPIOx will go high if the charger is active. The gpioX_mode should be set to output.

EOC output

When selected, the GPIOx will go high if the charger has reached the EOC state. The gpioX_mode should be set to output.

100/500mA charger input

With this function the charger input current limiter can be set to 100 or 500mA (low power or high power USB limit). The gpioX_mode should be set to input.

500/2.5A charger input

With this function the charger input current limiter can be set to 500 or 2.5A (high power USB limit or full current enabled). The gpioX_mode should be set to input.

Charging enable input

When pulling the GPIO to high the charger is being enabled and vice versa. This is to enable the charger without I^2C communication. The gpioX_mode should be set to input.

PWM output

The gpio block includes an internal programmable PWM generator (can be connected to any of the GPIO outputs). Its timing is defined by pwm_h_time, pwm_l_time and pwm_div. The gpioX_mode should be set to output.

Parameter

Figure 59:
GPIO Pin Characteristics
V_{VSUP}=2.7 to 5.5V; T_{amb}= –20 to +70°C; unless otherwise specified

Symbol	Parameter	Note	Min	Typ	Max	Unit
$V_{GPIOMAX}$	Maximum voltage on GPIO1 to 4 pins	Pin VSUP_GPIO is used as supply for the GPIO pins			V_{VSUP_GPIO} + 0.3	V
V_{OL}	Low level output voltage	I_{OL}=+1mA; digital output	–0.3		+0.4	V
V_{OH}	High level output voltage	I_{OH}=–1mA; digital push-pull output	0.8.V_{VSUP_GPIO}		V_{VSUP_GPIO}	V
V_{IL}	Low level input voltage	Digital input	–0.3		0.4	V
V_{IH}	High level input voltage	Digital input	1.4		V_{VSUP_GPIO}	V
$I_{LEAKAGE}$	Leakage current	High impedance			10	µA
$R_{pull-up}$	Pull-up resistance	If enabled, VSUP_GPIO=3.6V		300		kΩ
$R_{pull-down}$	Pull-down resistance	Digital input; if enabled; VSUP_GPIO=3.6V		300		kΩ

Supervisor

All LDO's, the DCDC step ups and DCDC step downs have an integrated over-current protection.

An overtemperature protection of the chip is also integrated which can be switched ON with the serial interface signal temp_pmc_on (enabled by default; it is not recommended to disable the over-temperature protection).

Description

The chip has two signals for the serial interface: ov_temp_110 and ov_temp_140. The flag ov_temp_110 is automatically reset if the overtemperature condition is removed, whereas ov_temp_140 has to be reset by the serial interface with the signal rst_ov_temp_140.

If the flag ov_temp_140 is set, an automatic reset of the complete chip is initiated. The chip will only start-up when the temperature falls below the T_{110} level (including hysteresis).

The flag ov_temp_140 is not affected by this reset cycle allowing the software to detect the reason for this unexpected shutdown.

Figure 60:
Over-temperature Detection

Symbol	Parameter	Note	Min	Typ	Max	Unit
T_{110}	ov_temp_110 rising threshold		95	110	125	°C
T_{140}	ov_temp_140 rising threshold		125	140	155	°C
T_{hyst}	ov_temp_110 and ov_temp_140 hysteresis			5		°C

Watchdog

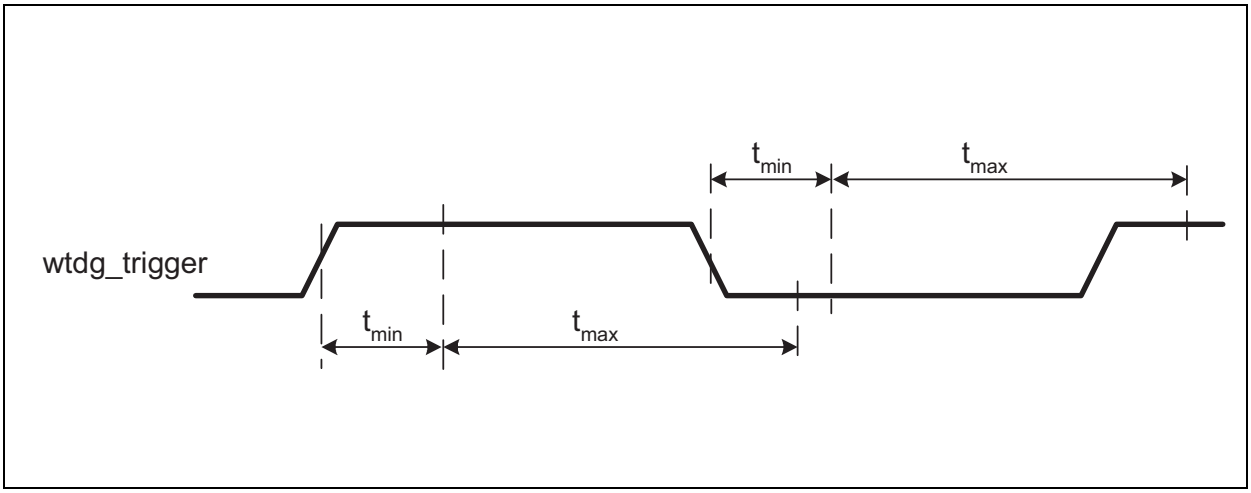
Description

The purpose of the watchdog is to detect a deadlock of the software. If the watchdog is active, it must receive a continuous trigger signal within a programmable time window. If there is no signal anymore for a certain time period from a defined pad or special serial interface bit, it starts either a complete reset cycle or changes the state of an output pin, which can be used e.g. as an interrupt to the processor.

- The watchdog is highly configurable by the following register bits:
- The complete block can be switched ON by wtdg_on = 1 and OFF by wtdg_on = 0.
- The watchdog time window is defined by the register wtdg_min_timer and wtdg_max_timer.
- The trigger signal can be configured by register wtdg_sw_sig and gpio1_iosf or gpio4_iosf.
- If the watchdog expires, the system can start automatically a reset cycle if wtdg_reset_on = 1.

Parameter

Figure 61:
Watchdog Timing Diagram



Interrupt Generation

Description

The interrupt controller generates an interrupt request for the host controller as soon as one or more of the bits in the Interrupt 1 to 3 register are set by pulling high pin INT (INT has to be selected as a GPIO output function). The output polarity can be changed to active low (XINT) by using the gpioX_invert bit of the selected GPIO. All the interrupt sources can be enabled in the Interrupt Mask 1 to 3 register. The Interrupt 1 to 3 registers are cleared automatically after the host controller has read them. To prevent the AS3711 device from losing an interrupt event, the register that is read is captured before it is transmitted to the host controller via the serial interface. As soon as the transmission of the captured value is complete a logical AND operation with the bit wise inverted captured value is applied to the register to clear all interrupt bits that have already been transmitted. Clearing the read interrupt bits takes 2 clock cycles, a read access to the same register before the clearing process has completed will yield a value of '0'. Note that an interrupt that has been present at the previous read access will be cleared as well in case it occurs again before the clearing process has completed.

During a read access to one of the interrupt registers the INT pin will be released. As soon as the transferred bits of the interrupt register have been cleared the INT pin will be pulled high in case a new interrupt has occurred in the meantime. By doing so the interrupt controller will work correctly with host controllers that are edge- and level-sensitive on their interrupt request input. Multiple byte read access is recommended to avoid reading the Interrupt 1 register over and over again in response to a new interrupt that has occurred in the same register (and thus pulling high pin INT) before the Interrupt 2,3 register has been read.

10-Bit ADC

This general purpose ADC can be used for measuring several voltages and currents to perform functions like battery monitor, temperature supervision, button press detection, etc.

Input Sources

Figure 62:
ADC10 Input Sources

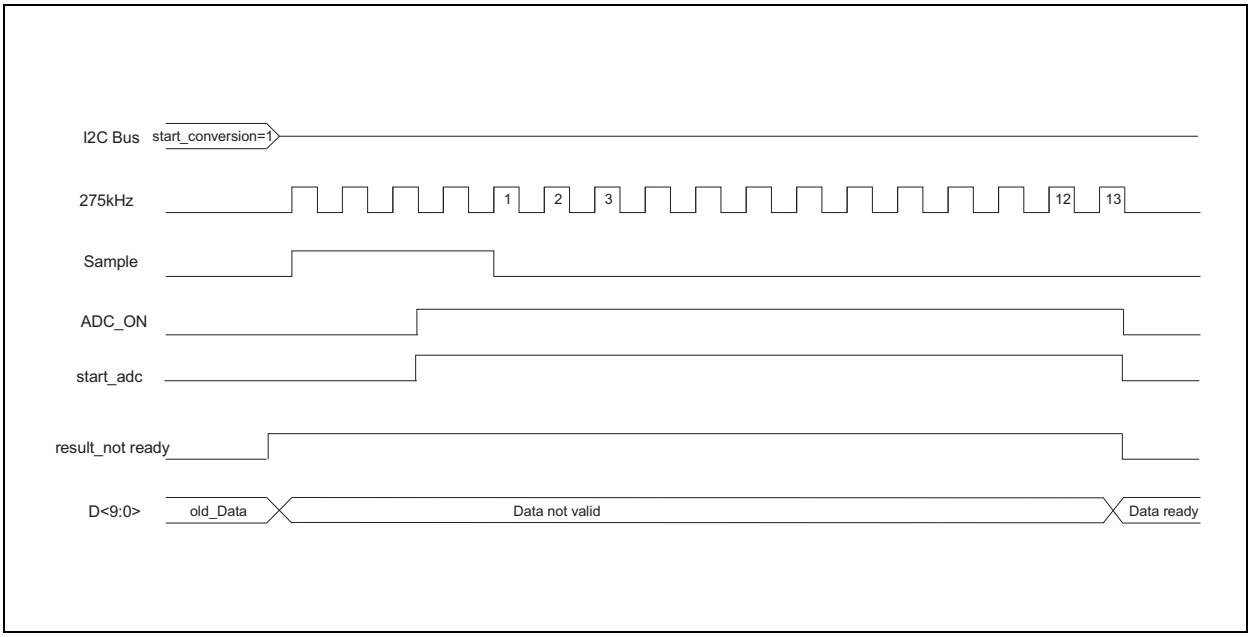
#	Source	Range	LSB	Mode	Description
0	BATTEMP	1.8V	1.76mV	1:1	Check battery charging temperature
1	DIE temperature	1.8V	1.76mV	1:1	Tj = (0.866 * ADC10<9:0>) -274
2	XOUT32X	1.8V	1.76mV	1:1	
3	CURR1	1.0V	1.76mV	1:1	
4	CURR2	1.0V	1.76mV	1:1	
5	CURR3	1.0V	1.76mV	1:1	
6	VUSB	15V	26.4mV	15:1	check USB charger HV input
7	CHGIN	5.5V	7.03mV	4:1	check USB charger LV input
8	VBAT	5.5V	7.03mV	4:1	check Li-Ion battery voltage
9	VSUP	5.5V	7.03mV	4:1	check main system supply voltage
A	SENSEN_SU1	1.8V / 5.5V	1.76 / 7.03mV	1:1 / 4:1	
B	LX_SD4	1.8V / 5.5V	1.76 / 7.03mV	1:1 / 4:1	
C	GPIO2	1.8V / 5.5V	1.76 / 7.03mV	1:1 / 4:1	
D	GPIO3	1.8V / 5.5V	1.76 / 7.03mV	1:1 / 4:1	
E	GPIO4	1.8V / 5.5V	1.76 / 7.03mV	1:1 / 4:1	
F					Reserved

Parameter

Figure 63:
ADC Characteristics

Symbol	Parameter	Note	Min	Typ	Max	Unit
	Resolution		10			Bit
V_{IN}	Input Voltage Range	For 1:1 mode	0		1.8	V
DNL	Differential Nonlinearity	1LSB 1.76mV for 1:1 (depending on selected channel)		±0.25		LSB
INL	Integral Nonlinearity			±0.5		LSB
Vos	Input Offset Voltage			2		LSB
R_{IN}	Input Impedance	4:1 mode	200			kΩ
		1:1 mode	100			MΩ
C_{IN}	Input Capacitance			3	9	pF
I_{DD}	Power Supply Current	During conversion only		500		µA
I_{DD}	Power Down Current			100		nA
Transient Parameters (25°C)						
Tc	Conversion Time			40		µs
fc	Clock Frequency	Internal CLK frequency/8		f_{clk_int} /8		kHz
ts	Settling time of S&H		1			µs

Figure 64:
ADC Timing-diagram



Real Time Clock

Description

The RTC is only available in QFN56 package. The RTC module provides time information to the system. It is implemented as a 6-bit counter that is incremented every second - with the 32kHz oscillator delivering the necessary accurate time base – and is reset to 0 each time the counter value is 60. An additional 24-bit minute counter is incremented each time the 6-bit counter is reset to 0. Both counters are set to 0 at a power-on-reset. The host controller can set the counter to any value by setting the RTC 1 to 4 registers.

To prevent ambiguous time information because of the 30-bit value being incremented before all of the 4 registers have been read or written, a 30-bit parallel shadow register is implemented. Every time a write/read access via the serial interface occurs the parallel shadow register is updated with the current value of the 30-bit counter. Any write access to the RTCSecond register will disable the update of the parallel register and set the value of the appropriate byte of the parallel register. Any subsequent write access to the RTCMinute3 register will transfer the current value of the 30-bit parallel register to the RTCSecond/Minute1 to 3 registers and the update of the parallel register is enabled again. Similarly, any read access to the RTCSecond register will freeze the current value of the parallel register and submit the appropriate byte to the host controller via the serial interface. Any subsequent read access to the RTCMinute3 register will enable the update of the parallel register again. This mechanism makes sure that the maximum error of the value that is written to or read from the registers is 1 second.

To start the RTC, rtc_on bit has to be set to 1.

The RTC stops automatically at its highest value (3B,FF,FF,FF) to prevent overrun.

Alarm

The RTC module includes an alarm function. When the content of the RTCAlarm registers equals the content of the RTC registers bit rtc_alarm will be set in the interrupt register. Furthermore the RTC module can generate a repeating interrupt every second, every minute, every 2 minutes or every 8 minutes.

To avoid ambiguous behavior during write access to the RTCAlarm registers any write access to the RTCAlarmSecond register will disable the alarm function; any subsequent write access to the RTCAlarmMinute3 will enable the alarm function again.

2-Wire-Serial Control Interface

Feature List

- Fast-mode capability (max. SCL-frequency is 400 kHz)
- 7+1-bit addressing mode
- 60h x 8-bit data registers (word address 0x00 - 0x60)
- Write formats: Single-Byte-Write, Page-Write
- Read formats: Current-Address-Read, Random-Read, Sequential-Read
- SDA input delay and SCL spike filtering by integrated RC-components

Protocol

Figure 65:
2-Wire Serial Symbol Definition

Symbol	Definition	RW	Note
S	Start condition after stop	R	1 bit
Sr	Repeated start	R	1 bit
DW	Device address for write	R	1000 0000b (80h)
DR	Device address for read	R	1000 0001b (81h)
WA	Word address	R	8 bit
A	Acknowledge	W	1 bit
N	No Acknowledge	R	1 bit
reg_data	Register data/write	R	8 bit
data (n)	Register data/read	W	8 bit
P	Stop condition	R	1 bit
WA++	Increment word address internally	R	During acknowledge

Figure 66:
Byte Write

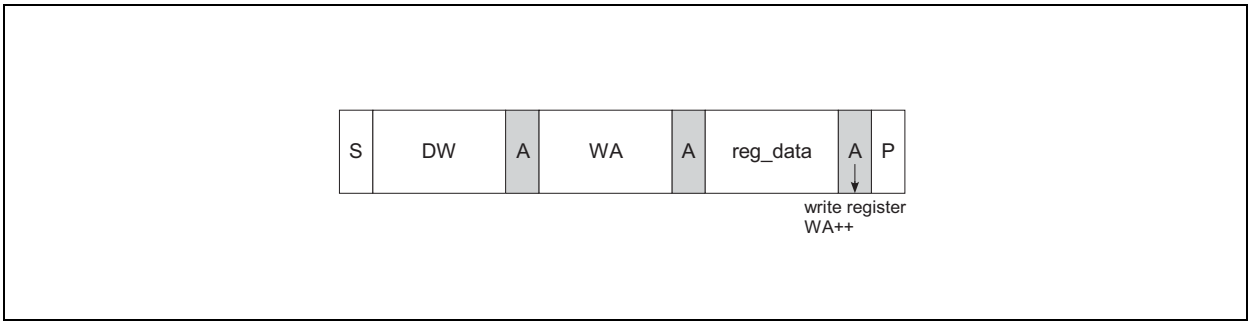
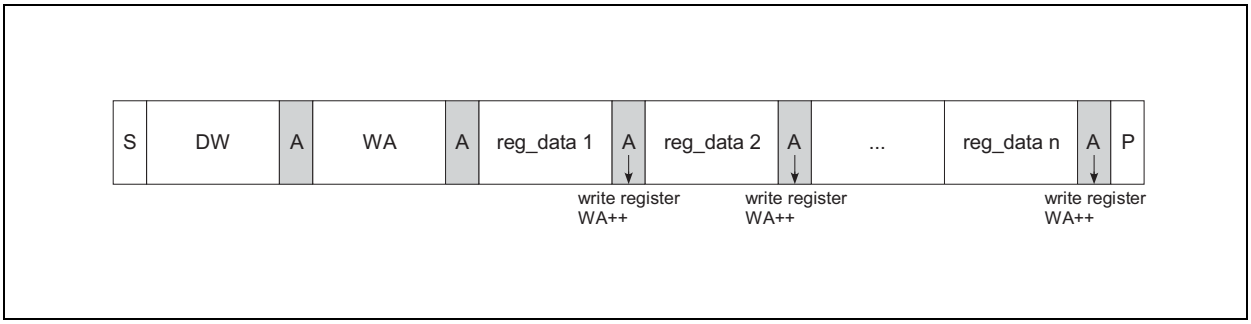


Figure 67:
Page Write

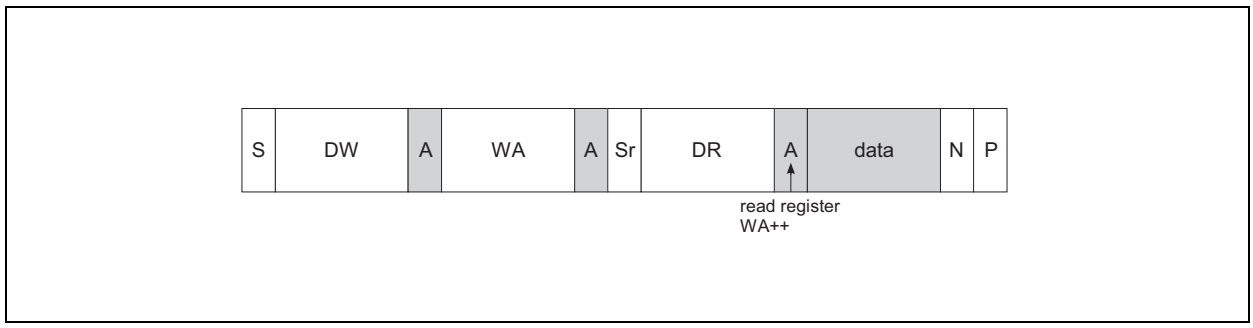


Byte Write and Page Write formats are used to write data to the slave.

The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The devicewrite address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

Figure 68:
Random Read

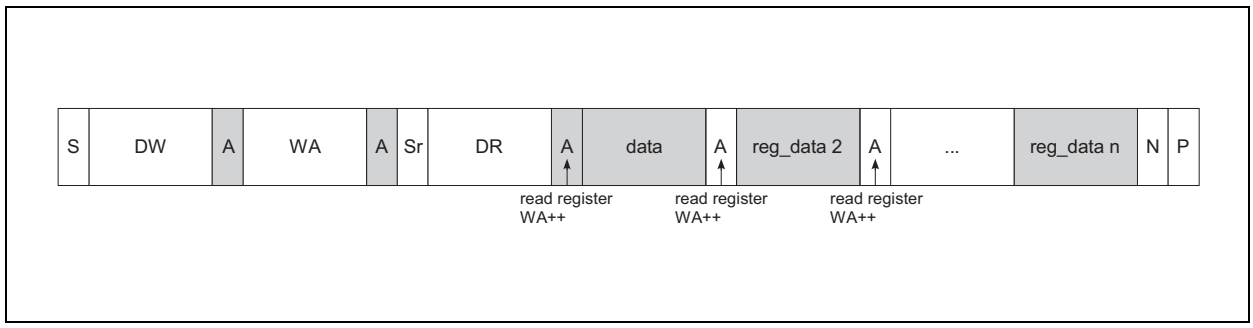


Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

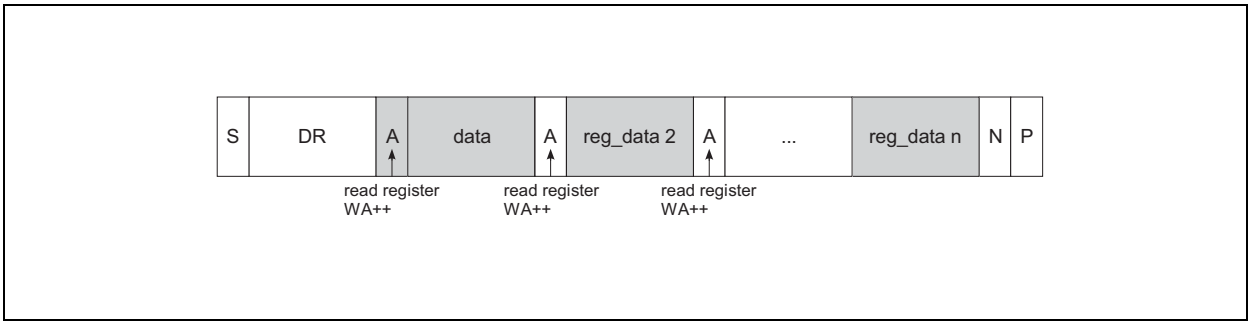
In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

Figure 69:
Sequential Read



Sequential Read is the extended form of Random Read, as more than one register-data bytes are transferred subsequently. In difference to the Random Read, for a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

Figure 70:
Current Address Read



To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer.

The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes has to be responded with an acknowledge from the master. For termination of the transmission the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.

Parameter

Figure 71:
I^2C SDA,SCL Characteristics

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{IL}	SCL,SDA Low Level input voltage		-0.3		0.4	V
V_{IH}	SCL,SDA High Level input voltage		1.4		VSUP_GPIO	V

Register Overview

Figure 72:
Register Overview

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
00h	SD1Voltage	sd1_frequ	sd1_vsel<6:0>						
01h	SD2Voltage	sd2_frequ	sd2_vsel<6:0>						
02h	SD3Voltage	sd3_frequ	sd3_vsel<6:0>						
03h	SD4Voltage		sd4_vsel<6:0>						
04h	LDO1Voltage	ldo1_on	ldo1_ilimit	-	ldo1_vsel<4:0>				
05h	LDO2Voltage	ldo2_on	ldo2_ilimit	-	ldo2_vsel<4:0>				
06h	LDO3Voltage	ldo3_on	ldo3_ilimit	ldo3_vsel<5:0>					
07h	LDO4Voltage	ldo4_on	ldo4_ilimit	ldo4_vsel<5:0>					
08h	LDO5Voltage	ldo5_on	ldo5_ilimit	ldo5_vsel<5:0>					
09h	LDO6Voltage	ldo6_on	ldo6_ilimit	ldo6_vsel<5:0>					
0ah	LDO7Voltage	ldo7_on	ldo7_ilimit	ldo7_vsel<5:0>					
0bh	LDO8Voltage	ldo8_on	ldo8_ilimit	ldo8_vsel<5:0>					
0ch	GPIO1control	gpio1_invert	gpio1_iosf<6:3>				gpio1_mode<2:0>		
0dh	GPIO2control	gpio2_invert	gpio2_iosf<6:3>				gpio2_mode<2:0>		
0eh	GPIO3control	gpio3_invert	gpio3_iosf<6:3>				gpio3_mode<2:0>		
0fh	GPIO4control	gpio4_invert	gpio4_iosf<6:3>				gpio4_mode<2:0>		

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
10h	SD_control	-				sd4_enable	sd3_enable	sd2_enable	sd1_enable
20h	GPIOsignal_out	-				gpio4_out	gpio3_out	gpio2_out	gpio1_out
21h	GPIOsignal_in	-				gpio4_in	gpio3_in	gpio2_in	gpio1_in
22h	Reg1_Voltage	reg1_voltage<7:0>							
23h	Reg2_Voltage	reg2_voltage<7:0>							
24h	Reg_control	reg2_select<7:4>				reg1_select<3:0>			
25h	GPIOctrl_sd	gpio_ctrl_sd4<7:6>		gpio_ctrl_sd3<5:4>		gpio_ctrl_sd2<3:2>		gpio_ctrl_sd1<1:0>	
26h	GPIOctrl_ldo1	gpio_ctrl_ldo4<7:6>		gpio_ctrl_ldo3<5:4>		gpio_ctrl_ldo2<3:2>		gpio_ctrl_ldo1<1:0>	
27h	GPIOctrl_ldo2	gpio_ctrl_ldo8<7:6>		gpio_ctrl_ldo7<5:4>		gpio_ctrl_ldo6<3:2>		gpio_ctrl_ldo5<1:0>	
2bh	Reg3_Voltage	reg3_voltage<7:0>							
2ch	Reg_control3	-				reg3_select<3:0>			
30h	SD_control1	sd4_low_noise	sd3_low_noise	sd2_low_noise	sd1_low_noise	sd4_fast	sd3_fast	sd2_fast	sd1_fast
31h	SD_control2	sd_dvm_select<7:6>		dvm_time<5:4>		sd3_slave	sd3_fsel	sd2_fsel	sd1_fsel
32h	Battery_voltage_monitor	FastResEn	SupResEn	ResVoltFall<5:3>			ResVoltRise<2:0>		
33h	Startup_Control				-			chg_pwr_off_en	power_off_at_vsuplow
34h	ResetTimer	-	stby_reset_disable	auto_off	off_delay<4:3>		-	res_timer<1:0>	
35h	ReferenceControl	on_reset_delay	reg_low_bias_mode	clk_div2	standby_mode_on	clk_int<3:1>			low_power_on

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
36h	ResetControl	onkey_reset	reset_reason<6:3>				on_input	power_off	force_reset
37h	Overtemperature Control					rst_ov_temp_140	ov_temp_140	ov_temp_110	temp_pmc_on
38h	WatchdogControl	-						wtdg_res_on	wtdg_on
39h	Reg_standby_mod1	disable_regpd	-			sd4_stby_on	sd3_stby_on	sd2_stby_on	sd1_stby_on
3ah	Reg_standby_mod2	ldo8_stby_on	ldo7_stby_on	ldo6_stby_on	ldo5_stby_on	ldo4_stby_on	ldo3_stby_on	ldo2_stby_on	ldo1_stby_on
40h	curr_control	curr3_ctrl<7:4>				curr2_ctrl<3:2>		curr1_ctrl<1:0>	
41h	pwm_control_l	pwm_l_time<7:0>							
42h	pwm_control_h	pwm_h_time<7:0>							
43h	curr1_value	curr1_current<7:0>							
44h	curr2_value	curr2_current<7:0>							
45h	curr3_value	curr3_current<7:0>							
46h	Watchdog_min_timer	wtdg_min_timer<7:0>							
47h	Watchdog_max_timer	wtdg_max_timer<7:0>							
48h	WatchdogSoftwareSignal	pwm_div<7:6>		-					wtdg_sw_sig
50h	Stepup_control1	stepup1_v<7:3>					stepup1_res	stepup1_freq	stepup1_on

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
51h	Stepup_control2	stepup2_v<7:3>					stepup2_res	stepup2_freq	stepup2_on
53h	Stepup_control4	stpup1_det	stpup1_oc	stpup1_oc_timeout	stpup1_shortprot	stpup2_pwm_lowf	stepup2_prot_dis	stepup2_fb<1:0>	
54h	Stepup_control5	-				stepup2_pwm_mode	stepup12_clkinv	stepup2_fbprot <1:0>	
60h	RTCcontrol			-	rtc_irq_mode<4:3>		rtc_on	rtc_alarm_wakeup_en	rtc_rep_wakeup_en
61h	RTCSecond	second<7:0>							
62h	RTCMinute1	minute0<7:0>							
63h	RTCMinute2	minute1<7:0>							
64h	RTCMinute3	minute2<7:0>							
65h	RTCAlarmSecond	alarmsecond<7:0>							
66h	RTCAlarmMinute1	alarmminute0<7:0>							
67h	RTCAlarmMinute2	alarmminute1<7:0>							
68h	RTCAlarmMinute3	alarmminute2<7:0>							
69h	SRAM	SRAM<7:0>							
70h	ADC_control	start_conversion	adc_on	adc_slow	gpio_lv	adc_select<3:0>			
71h	ADC_MSB_result	result_not_ready	D9_3<6:0>						
72h	ADC_LSB_result	-					D2_0<2:0>		

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
73h	RegStatus	curr3_lv	curr2_lv	curr1_lv	-	sd4_lv	sd3_lv	sd2_lv	sd1_lv
74h	InterruptMask1	LowBat_int_m	ovtmp_int_m	onkey_int_m	chdet_int_m	eoc_int_m	resume_int_m	nobat_int_m	trickle_int_m
75h	InterruptMask2	rtc_rep_int_m	stpup1_det_m	stpup1_oc_m	bat_temp_m	sd4_lv_int_m	sd3_lv_int_m	sd2_lv_int_m	sd1_lv_int_m
76h	InterruptMask3	-					gpio_restart_int_m	gpio_int_m	rtc_alarm_int_m
77h	InterruptStatus1	LowBat_int_i	ovtmp_int_i	onkey_int_i	chdet_int_i	eoc_int_i	resume_int_i	nobat_int_i	trickle_int_i
78h	InterruptStatus2	rtc_rep_int_i	stpup1_det_i	stpup1_oc_i	bat_temp_i	sd4_lv_int_i	sd3_lv_int_i	sd2_lv_int_i	sd1_lv_int_i
79h	InterrupStatus3	-					gpio_restart_int_i	gpio_int_i	rtc_alarm_int_i
80h	ChargerControl1	nobat_ntc_det	auto_resume	bat_charging_enable	usb_current<4:1>				usb_chgEn
81h	ChargerVoltageControl	vsup_min<7:6>		ChVoltEOC<5:0>					
82h	ChargerCurrentControl	eoc_current	cc_lowlimit	ConstantCurrent<5:2>				TrickleCurrent<1:0>	
83h	Chargerconfig	-	Charging_1Hz_clk	ChVoltResume	temp_sel<4:3>		vsup_voltage<2:0>		
84h	NTCsupervision	-					ntc_temp	ntc_10k	ntc_on
85h	Chargersupervision	-	ovprot_dis	dcdc_chmode	charging_tmax	ch_timeout<3:0>			
86h	ChargerStatus1	Nobat	Battemp_hi	EOC	CVM	Trickle	Resume	CCM	ChDet

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
87h	ChargerStatus2	-					usb_prot_ready	batsw_on	batsw_mode
8eh	LockRegister	-					charger_lock	reg_lock<1:0>	
90h	ASIC_ID1	ID1<7:0>							
91h	ASIC_ID2	-					revision<3:0>		

Figure 73:
SD1Voltage Register (Address 00h)

Addr: 00h		SD1Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	sd1_frequ	0	RW	Selects between high and low frequency dependent on sd1_fsel **0** : 2MHz if sd1_fsel =0, 3MHz if sd1_fsel =1 **1** : 3MHz if sd1_fsel =0, 4MHz if sd1_fsel =1
6:0	sd1_vsel	'b0000000	RW	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. **00h :** DC/DC powered down **01h-40h :** V_SD1=0.6V+sd1_vsel*12.5mV **41h-70h :** V_SD1=1.4V+(sd1_vsel-40h)*25mV **71h-7Fh :** V_SD1=2.6V+(sd1_vsel-70h)*50mV

Figure 74:
SD2Voltage Register (Address 01h)

Addr: 01h		SD2Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	sd2_frequ	0	RW	Selects between high and low frequency dependent on sd2_fsel **0** : 2MHz if sd2_fsel=0, 3MHz if sd2_fsel=1 **1** : 3MHz if sd2_fsel=0, 4MHz if sd2_fsel=1
6:0	sd2_vsel	'b0000000	RW	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. **00h** : DC/DC powered down **01h-40h** : V_SD2=0.6V+sd2_vsel*12.5mV **41h-70h** : V_SD2=1.4V+(sd2_vsel-40h)*25mV **71h-7Fh** : V_SD2=2.6V+(sd2_vsel-70h)*50mV

Figure 75:
SD3Voltage Register (Address 02h)

Addr: 02h		SD3Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	sd3_frequ	0	RW	Selects between high and low frequency dependent on sd3_fsel **0** : 2MHz if sd3_fsel=0, 3MHz if sd3_fsel=1 **1** : 3MHz if sd3_fsel=0, 4MHz if sd3_fsel=1
6:0	sd3_vsel	'b0000000	RW	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. **00h** : DC/DC powered down **01h-40h** : V_SD3=0.6V+ sd3_vsel*12.5mV **41h-70h** : V_SD3=1.4V+(sd3_vsel-40h)*25mV **71h-7Fh** : V_SD3=2.6V+(sd3_vsel-70h)*50mV

Figure 76:
SD4Voltage Register (Address 03h)

Addr: 03h		SD4Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	-	0	RW	-
6:0	sd4_vsel	'b0000000	RW	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. **00h** : DC/DC powered down **01h-40h** : V_SD4=0.6V+sd4_vsel*12.5mV **41h-70h** : V_SD4=1.4V+(sd4_vsel-40h)*25mV **71h-7Fh** : V_SD4=2.6V+(sd4_vsel-70h)*50mV

Figure 77:
LDO1Voltage Register (Address 04h)

Addr: 04h		LDO1Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ldo1_on	0	RW	Switch ON of LDO1 **0 :** LDO OFF **1 :** LDO ON
6	ldo1_ilimit	0	RW	Sets limit of LDO1 **0 :** 150mA limit **1 :** 250mA limit
4:0	ldo1_vsel	'b0 0000	RW	The voltage select bits set the LDO output voltage **0h-0Fh :** 1.2V + ldo1_vsel*50mV **10h-1Fh :** 1.8V + (ldo1_vsel-16)*100mV

Figure 78:
LDO2Voltage Register (Address 05h)

Addr: 05h		LDO2Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ldo2_on	0	RW	Switch ON of LDO2 **0 :** LDO OFF **1 :** LDO ON
6	ldo2_ilimit	0	RW	Sets limit of LDO2 **0 :** 150mA limit **1 :** 250mA limit
4:0	ldo2_vsel	'b0 0000	RW	The voltage select bits set the LDO output voltage **0h-0Fh** : 1.2V + ldo2_vsel*50mV **10h-1Fh** : 1.8V + (ldo2_vsel-16)*100mV

Figure 79:
LDO3Voltage Register (Address 06h)

Addr: 06h		LDO3Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ldo3_on	0	RW	Switch ON of LDO3 **0 :** LDO OFF **1 :** LDO ON
6	ldo3_ilimit	0	RW	Sets limit of LDO3 **0 :** 150mA operating range **1 :** 300mA operating range
5:0	ldo3_vsel	'b0 0000	RW	The voltage select bits set the LDO output voltage **00h-10h** : V_LDO3=0.9V+ldo3_vsel*50mV **11h-1fh** : do not use **20h-3Fh** : V_LDO3=1.75V+(ldo3_vsel-20h)*50mV

Figure 80:
LDO4Voltage Register (Address 07h)

Addr: 07h		LDO4Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ldo4_on	0	RW	Switch ON of LDO4 **0 :** LDO OFF **1 :** LDO ON
6	ldo4_ilimit	0	RW	Sets limit of LDO4 **0 :** 150mA operating range **1 :** 300mA operating range
5:0	ldo4_vsel	'b0 0000	RW	The voltage select bits set the LDO output voltage **00h-10h** : V_LDO4=0.9V+ldo4_vsel*50mV **11h-1fh** : Do not use **20h-3Fh** : V_LDO4=1.75V+(ldo4_vsel-20h)*50mV

Figure 81:
LDO5Voltage Register (Address 08h)

Addr: 08h		LDO5Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ldo5_on	0	RW	Switch ON of LDO5 **0 :** LDO OFF **1 :** LDO ON
6	ldo5_ilimit	0	RW	Sets limit of LDO5 **0 :** 150mA operating range **1 :** 300mA operating range
5:0	ldo5_vsel	'b0 0000	RW	The voltage select bits set the LDO output voltage **00h-10h** : V_LDO5=0.9V+ldo5_vsel*50mV **11h-1fh** : Do not use **20h-3Fh** : V_LDO5=1.75V+(ldo5_vsel-20h)*50mV

Figure 82:
LDO6Voltage Register (Address 09h)

Addr: 09h		LDO6Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ldo6_on	0	RW	Switch ON of LDO6 **0 :** LDO OFF **1 :** LDO ON
6	ldo6_ilimit	0	RW	Sets limit of LDO6 **0 :** 150mA operating range **1 :** 300mA operating range
5:0	ldo6_vsel	'b0 0000	RW	The voltage select bits set the LDO output voltage **00h-10h** : V_LDO6=0.9V+ldo6_vsel*50mV **11h-1fh** : Do not use **20h-3Fh** : V_LDO6=1.75V+(ldo6_vsel-20h)*50mV

Figure 83:
LDO7Voltage Register (Address 0ah)

Addr: 0ah		LDO7Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ldo7_on	0	RW	Switch ON of LDO7 **0 :** LDO OFF **1 :** LDO ON
6	ldo7_ilimit	0	RW	Sets limit of LDO7 **0 :** 150mA operating range **1 :** 300mA operating range
5:0	ldo7_vsel	'b0 0000	RW	The voltage select bits set the LDO output voltage **00h-10h** : V_LDO7=0.9V+ldo7_vsel*50mV **11h-1fh** : Do not use **20h-3Fh** : V_LDO7=1.75V+(ldo7_vsel-20h)*50mV

Figure 84:
LDO8Voltage Register (Address 0bh)

Addr: 0bh		LDO8Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ldo8_on	0	RW	Switch ON of LDO8 **0 :** LDO OFF **1 :** LDO ON
6	ldo8_ilimit	0	RW	Sets limit of LDO8 **0 :** 150mA operating range **1 :** 300mA operating range
5:0	ldo8_vsel	'b0 0000	RW	The voltage select bits set the LDO output voltage **00h-10h** : V_LDO8=0.9V+ldo8_vsel*50mV **11h-1fh** : Do not use **20h-3Fh** : V_LDO8=1.75V+(ldo8_vsel-20h)*50mV

Figure 85:
GPIO1control Register (Address 0ch)

Addr: 0ch		GPIO1control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio1_invert	0	RW	Invert GPIO input/output **0 :** Normal mode **1 :** Invert input or output
6:3	gpio1_iosf	'b0000	RW	Select the GPIO special function **0 :** Normal I/O operation **1 :** Interrupt output **2 :** VSUP_low output **3 :** GPIO interrupt input **4 :** Current sink PWM input **5 :** Vselect input, (apply on reg1_select, reg2_select and reg3_select, if gpio2_iosf=5 then apply on reg1_select only) **6 :** standby + Vselect + restart interrupt input **7 :** pwr_good output **8 :** Q32k output (if rtc_on=0 then internal RC oscillator with 32kHz divider is used) **9 :** Watchdog input **10 :** Charger active output **11 :** EOC output **12 :** 100/500mA charger input **13 :** 500mA/2.5A charger input **14 :** PWM output **15 :** Charger enable input
2:0	gpio1_mode	'b011	RW	Selects the GPIO mode (I, I/O, Tri, Pulls) **0 :** Input **1 :** Output (push and pull) **2 :** IO (open drain, only NMOS is active) **3 :** Tristate **4 :** Input with pullup **5 :** Input with pulldown **6 :** IO (open drain (NMOS) with pullup) **7 :** n/a

Figure 86:
GPIO2control Register (Address 0dh)

Addr: 0dh		GPIO2control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio2_invert	0	RW	Invert GPIO input/output **0 :** Normal mode **1 :** Invert input or output
6:3	gpio2_iosf	'b0000	RW	Select the GPIO special function **0 :** Normal I/O operation **1 :** Interrupt output **2 :** VSUP_low output **3 :** GPIO interrupt input **4 :** Current sink PWM input **5 :** Vselect input, (apply on reg1_select, reg2_select and reg3_select, if gpio1_iosf=5 then apply on reg2_select and reg3_select only) **6 :** standby + Vselect + restart interrupt input **7 :** pwr_good output **8 :** Q32k output (if rtc_on=0 then internal RC oscillator with 32kHz divider is used) **9 :** Stepup1 over-current output **10 :** Charger active output **11 :** EOC output **12 :** 100/500mA charger input **13 :** 500mA/2.5A charger input **14 :** PWM output **15 :** Charger enable input
2:0	gpio2_mode	'b011	RW	Selects the GPIO mode (I, I/O, Tri, Pulls) **0 :** Input **1 :** Output (push and pull) **2 :** IO (open drain, only NMOS is active) **3 :** ADC input (tristate) **4 :** Input with pullup **5 :** Input with pulldown **6 :** IO (open drain (NMOS) with pullup) **7 :** ADC input with pulldown

Figure 87:
GPIO3control Register (Address 0eh)

Addr: 0eh		GPIO3control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio3_invert	0	RW	Invert GPIO input/output **0 :** Normal mode **1 :** Invert input or output
6:3	gpio3_iosf	'b0000	RW	Select the GPIO special function **0 :** Normal I/O operation **1 :** Interrupt output **2 :** VSUP_low output **3 :** GPIO interrupt input **4 :** Current sink PWM input **5 :** Vselect input, (apply on reg1_select, reg2_select and reg3_select) **6 :** standby + Vselect + restart interrupt input **7 :** pwr_good output **8 :** Q32k output (if rtc_on=0 then internal RC oscillator with 32kHz divider is used) **9 :** Stepup1 over-current output **10 :** Charger active output **11 :** EOC output **12 :** 100/500mA charger input **13 :** 500mA/2.5A charger input **14 :** PWM output **15 :** Charger enable input
2:0	gpio3_mode	'b011	RW	Selects the GPIO mode (I, I/O, Tri, Pulls) **0 :** Input **1 :** Output (push and pull) **2 :** IO (open drain, only NMOS is active) **3 :** ADC input (tristate) **4 :** Input with pullup **5 :** Input with pulldown **6 :** IO (open drain (NMOS) with pullup) **7 :** ADC input with pulldown

Figure 88:
GPIO4control Register (Address 0fh)

Addr: 0fh		GPIO4control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio4_invert	0	RW	Invert GPIO input/output **0 :** Normal mode **1 :** Invert input or output
6:3	gpio4_iosf	'b0000	RW	Select the GPIO special function **0 :** Normal I/O operation **1 :** Interrupt output **2 :** VSUP_low output **3 :** GPIO interrupt input **4 :** Current sink PWM input **5 :** Vselect input, (apply on reg1_select, reg2_select and reg3_select) **6 :** standby + Vselect + restart interrupt input **7 :** pwr_good output **8 :** Q32k output (if rtc_on=0 then internal RC oscillator with 32kHz divider is used) **9 :** Watchdog input **10 :** Charger active output **11 :** EOC output **12 :** 100/500mA charger input **13 :** 500mA/2.5A charger input **14 :** PWM output **15 :** Charger enable input
2:0	gpio4_mode	'b011	RW	Selects the GPIO mode (I, I/O, Tri, Pulls) **0 :** Input **1 :** Output (push and pull) **2 :** IO (open drain, only NMOS is active) **3 :** ADC input (tristate) **4 :** Input with pullup **5 :** Input with pulldown **6 :** IO (open drain (NMOS) with pullup) **7 :** ADC input with pulldown

Figure 89:
SD_control Register (Address 10h)

Addr: 10h		SD_control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	-	'b0000	n/a	Do not use
3	sd4_enable	'b1	RW	Global stepdown4 enable **0 :** SD4 OFF **1 :** SD4 ON
2	sd3_enable	'b1	RW	Global stepdown3 enable **0 :** SD3 OFF **1 :** SD3 ON
1	sd2_enable	'b1	RW	Global stepdown2 enable **0 :** SD2 OFF **1 :** SD2 ON
0	sd1_enable	'b1	RW	Global stepdown1 enable **0 :** SD1 OFF **1 :** SD1 ON

Figure 90:
GPIOsignal_out Register (Address 20h)

Addr: 20h		GPIOsignal_out		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	-	'b0000	n/a	Do not use
3	gpio4_out	0	RW	This bit determines the output signal of the GPIO4 pin when selected as output source.
2	gpio3_out	0	RW	This bit determines the output signal of the GPIO3 pin when selected as output source.
1	gpio2_out	0	RW	This bit determines the output signal of the GPIO2 pin when selected as output source.
0	gpio1_out	0	RW	This bit determines the output signal of the GPIO1 pin when selected as output source.

Figure 91:
GPIOsignal_in Register (Address 21h)

Addr: 21h		GPIOsignal_in		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	-	'b0000	n/a	Do not use
3	gpio4_in	0	RO	This bit reflects the logic level of the GPIO4 pin when configured as digital input pin.
2	gpio3_in	0	RO	This bit reflects the logic level of the GPIO3 pin when configured as digital input pin.
1	gpio2_in	0	RO	This bit reflects the logic level of the GPIO2 pin when configured as digital input pin.
0	gpio1_in	0	RO	This bit reflects the logic level of the GPIO1 pin when configured as digital input pin.

Figure 92:
Reg1_Voltage Register (Address 22h)

Addr: 22h		Reg1_Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	reg1_voltage	'b0000 0000	RW	This register is mapped to the register address 0h+Reg1_select , if gioX_iosf = 5 or 6 (Vselect input), and the GPIOx input = 1. This feature allows voltage switching of a predefined regulator with just one GPIO input. **0 ..FFh** : Selects voltage, ilimit, on or frequency bits of LDO or DCDC

Figure 93:
Reg2_Voltage Register (Address 23h)

Addr: 23h		Reg2_Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	reg2_voltage	'b0000 0000	RW	This register is mapped to the register address 0h+Reg3_select , if gioX_iosf=5 or 6 (Vselect input), and GPIOx input = 1, This feature allows voltage switching of a predefined regulator with just one GPIO input **0 ..FFh** : Selects voltage, ilimit, on or frequency bits of LDO or DCDC

Figure 94:
Reg_control Register (Address 24h)

Addr: 24h		Reg_Control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	reg2_select	'b1111	RW	Selects regulator for mapping feature; if reg_select2 ≥ 0Ch, then feature is disabled.
3:0	reg1_select	'b1111	RW	Selects regulator for mapping feature; if reg_select1 ≥ 0Ch, then feature is disabled.

Figure 95:
GPIOctrl_sd Register (Address 25h)

Addr: 25h		GPIOctrl_sd		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	gpio_ctrl_sd4	'b00	RW	Enable GPIO control of DCDC SD4. GPIO ctrl only enabled, if sd4_vsel > 0 **0 :** No GPIO control **1 :** Controlled by GPIO1 **2 :** Controlled by GPIO2 **3 :** Controlled by GPIO3
5:4	gpio_ctrl_sd3	'b00	RW	Enable GPIO control of DCDC SD3. GPIO ctrl only enabled, if sd3_vsel > 0 **0 :** No GPIO control **1 :** Controlled by GPIO1 **2 :** Controlled by GPIO2 **3 :** Controlled by GPIO3
3:2	gpio_ctrl_sd2	'b00	RW	Enable GPIO control of DCDC SD2. GPIO ctrl only enabled, if sd2_vsel > 0 **0 :** No GPIO control **1 :** Controlled by GPIO1 **2 :** Controlled by GPIO2 **3 :** Controlled by GPIO3
1:0	gpio_ctrl_sd1	'b00	RW	Enable GPIO control of DCDC SD1. GPIO ctrl only enabled, if sd1_vsel > 0 **0 :** No GPIO control **1 :** Controlled by GPIO1 **2 :** Controlled by GPIO2 **3 :** Controlled by GPIO3

Figure 96:
GPIOctrl_ldo1 Register (Address 26h)

Addr: 26h		GPIOctrl_ldo1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	gpio_ctrl_ldo4	'b00	RW	Enable GPIO control of LDO4. GPIO ctrl only enabled, if ldo4_on = 1 **0 :** No GPIO control **1 :** Controlled by GPIO1 **2 :** Controlled by GPIO2 **3 :** Controlled by GPIO3
5:4	gpio_ctrl_ldo3	'b00	RW	Enable GPIO control of LDO3. GPIO ctrl only enabled, if ldo3_on = 1 **0 :** No GPIO control **1 :** Controlled by GPIO1 **2 :** Controlled by GPIO2 **3 :** Controlled by GPIO3
3:2	gpio_ctrl_ldo2	'b00	RW	Enable GPIO control of LDO2. GPIO ctrl only enabled, if ldo2_on = 1 **0 :** No GPIO control **1 :** Controlled by GPIO1 **2 :** Controlled by GPIO2 **3 :** Controlled by GPIO3
1:0	gpio_ctrl_ldo1	'b00	RW	Enable GPIO control of LDO1. GPIO ctrl only enabled, if ldo1_on = 1 **0 :** No GPIO control **1 :** Controlled by GPIO1 **2 :** Controlled by GPIO2 **3 :** Controlled by GPIO3

Figure 97:
GPIOctrl_ldo2 Register (Address 27h)

Addr: 27h		GPIOctrl_ldo2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	gpio_ctrl_ldo8	'b00	RW	Enable GPIO control of LDO8. GPIO ctrl only enabled, if ldo8_on = 1 **0 :** No GPIO control **1 :** Controlled by GPIO1 **2 :** Controlled by GPIO2 **3 :** Controlled by GPIO3
5:4	gpio_ctrl_ldo7	'b00	RW	Enable GPIO control of LDO7. GPIO ctrl only enabled, if ldo7_on = 1 **0 :** No GPIO control **1 :** Controlled by GPIO1 **2 :** Controlled by GPIO2 **3 :** Controlled by GPIO3
3:2	gpio_ctrl_ldo6	'b00	RW	Enable GPIO control of LDO6. GPIO ctrl only enabled, if ldo6_on = 1 **0 :** No GPIO control **1 :** Controlled by GPIO1 **2 :** Controlled by GPIO2 **3 :** Controlled by GPIO3
1:0	gpio_ctrl_ldo5	'b00	RW	Enable GPIO control of LDO5. GPIO ctrl only enabled, if ldo5_on = 1 **0 :** No GPIO control **1 :** Controlled by GPIO1 **2 :** Controlled by GPIO2 **3 :** Controlled by GPIO3

Figure 98:
Reg3_Voltage Register (Address 2bh)

Addr: 2bh		Reg3_Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	reg3_voltage	'b0000 0000	RW	This register is mapped to the register address 0h+Reg3_select , if gioX_iosf=5 or 6 (Vselect input), and GPIOx input = 1, This feature allows voltage switching of a predefined regulator with just one GPIO input **0 ..FFh** : Selects voltage, ilimit, on or frequency bits of LDO or DCDC

Figure 99:
Reg_control3 Register (Address 2ch)

Addr: 2ch		Reg3_Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	-	'b0000	n/a	Do not use
3:0	reg3_select	'b1111	RW	Selects regulator for mapping feature; if reg_select3 ≥ 0Ch, then feature is disabled.

Figure 100:
SD_control1 Register (Address 30h)

Addr: 30h		SD_control1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	sd4_low_noise	0	RW	Enables low noise mode of SD4. If enabled, smaller current pulses and output ripple is activated. **0 :** Normal mode. Minimum current pulses of >100mA applied in skip mode. **1 :** Low noise mode. Only minimum on time applied in skip mode.
6	sd3_low_noise	0	RW	Enables low noise mode of SD3. If enabled, smaller current pulses and output ripple is activated. **0 :** Normal mode. Minimum current pulses of >100mA applied in skip mode. **1 :** Low noise mode. Only minimum on time applied in skip mode.
5	sd2_low_noise	0	RW	Enables low noise mode of SD2. If enabled, smaller current pulses and output ripple is activated. **0 :** Normal mode. Minimum current pulses of >100mA applied in skip mode. **1 :** Low noise mode. Only minimum on time applied in skip mode.
4	sd1_low_noise	0	RW	Enables low noise mode of SD1. If enabled, smaller current pulses and output ripple is activated. **0 :** Normal mode. Minimum current pulses of >100mA applied in skip mode. **1 :** Low noise mode. Only minimum on time applied in skip mode.
3	sd4_fast	0	RW	Selects a faster regulation mode for SD4 suitable for larger load changes. **0 :** Normal mode **1 :** Fast mode, double Cext required (see external components)
2	sd3_fast	0	RW	Selects a faster regulation mode for SD3 suitable for larger load changes. **0 :** Normal mode **1 :** Fast mode, double Cext required (see external components)
1	sd2_fast	0	RW	Selects a faster regulation mode for SD2 suitable for larger load changes. **0 :** Normal mode **1 :** Fast mode, double Cext required (see external components)
0	sd1_fast	0	RW	Selects a faster regulation mode for SD1 suitable for larger load changes. **0 :** Normal mode **1 :** Fast mode, double Cext required (see external components)

Figure 101:
SD_control2 Register (Address 31h)

Addr: 31h		SD_control2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	sd_dvm_select	'b00	RW	Apply DVM counter to the following DCDC converter: **0 :** Select SD1 for DVM **1 :** Select SD2 for DVM **2 :** Select SD3 for DVM **3 :** Select SD4 for DVM
5:4	dvm_time	'b00	RW	Time steps of DVM voltage change of selected step down, if voltage of step Down is changed during operation (sdx_vsel) voltage is decreased/increased by single steps 12.5mV **0 :** 0 µsec, immediate change (no DVM) **1 :** 4 µsec time delay between steps **2 :** 8 µsec time delay between steps **3 :** 16 µsec time delay between steps
3	sd3_slave	0	RW	Enables slave mode of SD3 **0 :** Normal mode of SD3 **1 :** SD3 is slave of SD2
2	sd3_fsel	0	RW	Selects between high and low frequency range **0 :** 2 or 3MHz frequency (selectable by sd3_frequ) **1 :** 3 or 4MHz frequency (selectable by sd3_frequ)
1	sd2_fsel	0	RW	Selects between high and low frequency range **0 :** 2 or 3MHz frequency (selectable by sd2_frequ) **1 :** 3 or 4MHz frequency (selectable by sd2_frequ)
0	sd1_fsel	0	RW	Selects between high and low frequency range **0 :** 2 or 3MHz frequency (selectable by sd1_frequ) **1 :** 3 or 4MHz frequency (selectable by sd1_frequ)

Figure 102:
Battery_voltage_monitor Register (Address 32h)

Addr: 32h		Battery_voltage_monitor		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	FastResEn	0	RW	**0 :** ResVoltFall debounce time = 3msec **1 :** ResVoltFall debounce time = 49sec
6	SupResEn	0	RW	**0 :** A reset is generated if VSUP falls below 2.7V ** **1 :** A reset is generated if VSUP falls below ResVoltFall ** If VBAT falls below ResVoltFall only an interrupt is generated (if enabled) and the µProcessor can shut down the system)
5:3	ResVoltFall	'b000	RW	This value determines the reset level ResVoltFall for falling VBAT. It is recommended to set this value at least 200mV lower than ResVoltRise **0 :** 2.7V **1 :** 2.9V **2 :** 3.1V **3 :** 3.2V **4 :** 3.3V **5 :** 3.4V **6 :** 3.5V **7 :** 3.6V
2:0	ResVoltRise	'b000	RO (OTP)	This value determines the reset level ResVoltRise for rising VBAT. It is recommended to set this value at least 200mV higher than ResVoltFall **0 :** 2.7V **1 :** 2.9V **2 :** 3.1V **3 :** 3.2V **4 :** 3.3V **5 :** 3.4V **6 :** 3.5V **7 :** 3.6V

Figure 103:
Startup_Control Register (Address 33h)

Addr: 33h		Startup_Control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	-	'b00 0000	n/a	Do not use
1	chg_pwr_off_en	0	RO (OTP)	Select charger detection in power OFF mode Read only (OTP setting) **0 :** Exit of Power OFF mode, if charger is detected (level detection) **1 :** Exit of Power OFF mode, if charger insertion is detected (rising edge detection) .
0	power_off_at_vsupl ow	0	RW	Switch ON Power OFF mode if low VSUP is detected during active or standby mode (Pin ON= low and bit auto_off=0) **0 :** If low battery is detected, battery voltage is continuously monitored and chip startup initiated if battery voltage is above ResVoltRise **1 :** If low battery is detected, enter power OFF mode

Figure 104:
ResetTimer Register (Address 34h)

Addr: 34h		ResetTimer		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	-	'b0	n/a	Do not use
6	stby_reset_disable	0	RW	Disable Reset output signal (pin XRES) in standby mode. **0 :** Normal mode, reset is active in standby mode **1 :** No reset in standby mode and during exit of standy mode
5	auto_off	0	RO	Defines startup behavior at first battery insertion **0 :** Startup of chip if VBAT>ResVoltRise **1 :** Enter power OFF mode (Startup with ON key or charger insertion)
4:3	off_delay	'b01	RW	Set Delay between I^2C command, GPIO or Reset signal for power_off, standby mode or reset and execution of that command. **0 :** No delay **1 :** 8 msec **2 :** 16 msec **3 :** 32 msec
2	-	'b0	n/a	Do not use
1:0	res_timer	'b00	RW	Set RESTime, after the last regulator has started **0 :** RESTIME = 10ms **1 :** RESTIME = 50ms **2 :** RESTIME = 100ms **3 :** RESTIME = 150ms

Figure 105:
ReferenceControl Register (Address 35h)

Addr: 35h		ReferenceControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	on_reset_delay	0	RW	Sets the ON reset delay time **0 :** 8 sec (if onkey_reset=1) **1 :** 4 sec (if onkey_reset=1)
6	reg_low_bias_mode	0	RW	Sets the ON reset delay time **0 :** Normal operation **1 :** Reduces the bias for the analog LDO1 and LDO2
5	clk_div2	0	RW	Divide internal clock oscillator by 2 to reduce quiescent current for low power operation **0 :** Normal mode **1 :** Internal clock frequency divided by two. All timings are increased by two. Switching frequency of all DCDC converters are divided by two. Reduced transient performance of DCDC converters.
4	standby_mode_on	0	RW	Setting to 1 sets the PMU into standby mode. All regulators are disabled except those regulators enabled by register Reg standby mode. XRES will be pulled to low. A normal startup of all regulators will be done with any interrupt (has to be enabled before entering standby mode). During this startup, regulators defined by Reg standby mode register are continuously ON.
3:1	clk_int	'b000	RW	Sets the internal CLK frequency f_{CLK} used for DCDCs, PWM, ... **0 :** 4 MHz (default) **1 :** 3.8 MHz **2 :** 3.6 MHz **3 :** 3.4 MHz **4 :** 3.2 MHz **5 :** 3.0 MHz **6 :** 2.8 MHz **7 :** 2.6 MHz All frequencies, timings and delays in this datasheet are based on 4MHz clk_int
0	low_power_on	0	RW	Enable low power mode of internal reference. **0 :** Standard mode **1 :** Low power mode -all specification except noise parameters are still valid. Iq reduced by approx. 30µA

Figure 106:
ResetControl Register (Address 36h)

Addr: 36h		ResetControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	onkey_reset	0	RW	**0 :** Reset after 4/8 seconds ON pressed disabled **1 :** Reset after 4/8 seconds ON pressed enabled
6:3	reset_reason	'b0000	RW	Flags to indicate to the software the reason for the last reset **0 :** V_{POR} has been reached (battery or charger insertion from scratch) **1 :** ResVoltFall was reached (battery voltage drop below 2.75V) **2 :** Software forced by force_reset **3 :** Software forced by power_off and ON was pulled high **4 :** Software forced by power_off and charger was detected **5 :** External triggered through the pin XRES **6 :** Reset caused by overtemperature T140 **7 :** Reset caused by watchdog **8 :** Reset caused by 4/8 seconds ON press **9 :** NA **10 :** Reset caused by RTC repeated wakeup or alarm wakeup **11 :** Reset caused by interrupt in standby mode **12 :** Reset caused by ON pulled high in standby mode
2	on_input	0	R_PUSH	**Read:** This flag represents the state of the ON pad directly **Write:** Setting to 1 resets the 4/8 sec. onkey_reset timer
1	power_off	0	RW	Setting to 1 starts a reset cycle, but waits after the Reg_off state for a rising edge on the pin ON or until the charger is detected.
0	force_reset	0	RW	Setting to 1 starts a complete reset cycle

Figure 107:
OvertemperatureControl Register (Address 37h)

Addr: 37h		OvertemperatureControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	-	'b0000	n/a	Do not use
3	rst_ov_temp_140	0	RW	If the over-temperature threshold 2 has been reached, the flag ov_temp_140 is set and a reset cycle is started. ov_temp_140 should be reset by writing 1 and afterward 0 to rst_ov_temp_140.
2	ov_temp_140	0	RO	Flag that the over-temperature threshold 2 (T140) has been reached -this flag is not reset by a over-temperature caused reset and has to be reset by rst_ov_temp_140.
1	ov_temp_110	0	RO	Flag that the over-temperature threshold 1 (T110) has been reached
0	temp_pmc_on	1	RO	Switch ON /OFF of temperature supervision; default: ON -all other bits are only valid if set to 1. Leave at 1, do not disable

Figure 108:
WatchdogControl Register (Address 38h)

Addr: 38h		WatchdogControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	-	'b00 0000	n/a	Do not use
1	wtdg_res_on	0	RW	If the watchdog expires and wtdg_res_on = 1 a reset cycle will be started
0	wtdg_on	0	RW	Switches ON the complete watchdog **0 :** Watchdog OFF **1 :** Watchdog enabled

Figure 109:
Reg_standby_mod1 Register (Address 39h)

Addr: 39h		Reg_standby_mod1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	disable_regpd	0	RW	This bit disables the pulldown of all regulators **0 :** Normal operation approx. 1kΩ pulldown of all regulators **1 :** Pulldown disabled >100kΩ of all regulators
6:4	-	b000	n/a	Do not use
3	sd4_stby_on	0	RW	Enable Step down 4 in standby mode
2	sd3_stby_on	0	RW	Enable Step down 3 in standby mode
1	sd2_stby_on	0	RW	Enable Step down 2 in standby mode
0	sd1_stby_on	0	RW	Enable Step down 1 in standby mode

Figure 110:
Reg_standby_mod2 Register (Address 3ah)

Addr: 3ah		Reg_standby_mod2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ldo8_stby_on	0	RW	Enable LDO8 in standby mode
6	ldo7_stby_on	0	RW	Enable LDO7 in standby mode
5	ldo6_stby_on	0	RW	Enable LDO6 in standby mode
4	ldo5_stby_on	0	RW	Enable LDO5 in standby mode
3	ldo4_stby_on	0	RW	Enable LDO4 in standby mode
2	ldo3_stby_on	0	RW	Enable LDO3 in standby mode
1	ldo2_stby_on	0	RW	Enable LDO2 in standby mode
0	ldo1_stby_on	0	RW	Enable LDO1 in standby mode

Figure 111:
curr_control Register (Address 40h)

Addr: 40h		curr_control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	curr3_ctrl	'b0000	RW	ON/OFF control of the pad CURR3 **0 :** Current sink is turned OFF **1 :** Current sink is active **2 :** Current sink is active and LED string connected to SU2. Required for automatic feedback selection. **3 :** Controlled by internal PWM generator, or external, if gpioX_iosf=4 **4 :** XINT output (active low interrupt output) **5 :** VSUP_low output **6 :** Charger active output **7 :** EOC output **8 :** Inverted signal of ON pin as output **9 :** Signal of ON pin as output **10:** Q32k output (if rtc_on=0 then internal RC oscillator with 32kHz divider is used) **11 :** PWM output **12 :** PWRGOOD output **13-15 :** NA
3:2	curr2_ctrl	'b00	RW	ON/OFF control of the pad CURR2 **0 :** Current sink is turned OFF **1 :** Current sink is active **2 :** Current sink is active and LED string connected to SU2. Required for automatic feedback selection. **3 :** Controlled by internal PWM generator, or external, if gpioX_iosf=4
1:0	curr1_ctrl	'b00	RW	ON/OFF control of the pad CURR1 **0 :** Current sink is turned OFF **1 :** Current sink is active **2 :** Current sink is active and LED string connected to SU2. Required for automatic feedback selection. **3 :** Controlled by internal PWM generator, or external, if gpioX_iosf=4

Figure 112:
pwm_control_l Register (Address 41h)

Addr: 41h		pwm_control_l		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	pwm_l_time	'b00000000	RW	This bit defines the low time of the PWM generator in 1MHz units. **0** : pwm_div * 1µsec **1** : pwm_div * 2µsec **2** : pwm_div * 3µsec ... : ... **255** : pwm_div * 256µsec

Figure 113:
pwm_control_h Register (Address 42h)

Addr: 42h		pwm_control_h		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	pwm_h_time	'b00000000	RW	This bit defines the high time of the PWM generator in 1MHz units. **0** : pwm_div * 1µsec **1** : pwm_div * 2µsec **2** : pwm_div * 3µsec ... : ... **255** : pwm_div * 256µsec

Figure 114:
curr1_value Register (Address 43h)

Addr: 43h		curr1_value		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	curr1_current	'b00000000	RW	Defines the current into CURR1, if enabled by curr1_ctrl **0** : Power down (default state) **1** : 0.1563mA (LSB) ... : ... **255** : 39.84mA

Figure 115:
curr2_value Register (Address 44h)

Addr: 44h		curr2_value		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	curr2_current	'b00000000	RW	Defines the current into CURR2, if enabled by curr2_ctrl **0** : Power down (default state) **1** : 0.1563mA (LSB) ... : ... **255** : 39.84mA

Figure 116:
curr3_value Register (Address 45h)

Addr: 45h		curr3_value		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	curr3_current	'b00000000	RW	Defines the current into CURR3, if enabled by curr3_ctrl **0** : Power down (default state) **1** : 0.1563mA (LSB) ... : ... **255** : 39.84mA

Figure 117:
Watchdog_min_timer Register (Address 46h)

Addr: 46h		Watchdog_min_timer		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	wtdg_min_timer	'b00000000	RW	Defines the minimum watchdog trigger time (LSB=7.5ms, range: 0 - 1.9s)

Figure 118:
Watchdog_max_timer Register (Address 47h)

Addr: 47h		Watchdog_max_timer		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	wtdg_max_timer	'b00000000	RW	Defines the maximum watchdog trigger time (LSB=7.5ms, range: 7.5ms - 1.9s), do not set to (00)h

Figure 119:
WatchdogSoftwareSignal Register (Address 48h)

Addr: 48h		WatchdogSoftwareSignal		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	pwm_div	'b00	RW	This bit defines the divider ratio of the prescaler for the PWM generator. **0** : Divide by 1 **1** : Divide by 2 **2** : Divide by 4 **3** : Divide by 16
0	wtdg_sw_sig	0	PUSH	Trigger input by the serial interface if gpioX_iosf<>9

Figure 120:
Stepup_control1 Register (Address 50h)

Addr: 50h		Stepup_control1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	stepup1_v	'b0000	RW	Defines the tuning current at FB_SU1 pin; **0 :** 0 µA **1 :** 1 µA **... :** ... **31 :** 31 µA
2	stepup1_res	0	RW	Gain selection for DCDC SU1 **0 :** If FB_SU1 is used with current feedback only (Only R1,C1 connected) **1 :** If FB_SU1 is used with external resistor divider (2 resistors)
1	stepup1_freq	0	RW	Selects SU1 frequency **0 :** 1 MHz **1 :** 0.5 MHz
0	stepup1_on	0	RW	ON/OFF control of SU1 **0 :** SU1 OFF **1 :** SU1 ON

Figure 121:
Stepup_control2 Register (Address 51h)

Addr: 51h		Stepup_control2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	stepup2_v	'b0000	RW	Defines the tuning current at FB_SU2 pin; **0 :** 0 µA **1 :** 1 µA **... :** ... **31 :** 31 µA
2	stepup2_res	0	RW	Gain selection for DCDC SU2 **0** : If DCDC is used with current feedback (CURR1,CURR2,CURR3) or if FB_SU2 is used with current feedback only (Only R1,C1 connected) **1** : If FB_SU2 is used with external resistor divider (2 resistors)
1	stepup2_freq	0	RW	Selects SU3 frequency **0 :** 1 MHz **1 :** 0.5 MHz
0	stepup2_on	0	RW	ON/OFF control of SU2 **0 :** SU2 OFF **1 :** SU2 ON

Figure 122:
Stepup_control4 Register (Address 53h)

Addr: 53h		Stepup_control4		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	stpup1_det	0	RO	SU1 detection status register **0 :** VRsense < V_{DETECT} for more than 1ms, and DCDC SU1 converter is in pulseskip for more than 1ms. **1 :** VRsense > V_{DETECT} for more than 1ms, or the DCDC SU1 converter is not in pulseskip for more than 1ms.
6	stpup1_oc	0	RO	SU1 overcurrent status bit **0 :** VRsense < $V_{OVCURRENT}$ **1 :** VRsense > $V_{OVCURRENT}$ for more than 5ms (latched state)
5	stpup1_oc_timeout	0	RW	Controls GPIOx switch-OFF, after overcurrent timeout (5ms) for DCDC SU1 **0 :** Disabled **1 :** Enabled
4	stpup1_shortprot	0	RW	Enables Protection and Detection circuit for DCDC SU1 **0 :** No protection and load detection **1 :** Short protection and load detection enabled
3	stpup2_pwm_lowf	0	RW	Selects PWM operation of SU2 **0 :** High frequency operation PWM>20kHz** **1 :** Low frequency PWM operation: stepup2_on and curr1 to 3_on (if PWM enabled) switched OFF during PWM low time ** Step_up switched ON all the time. (current sinks are not switched OFF (currX_on=1 all the time), but currX_current masked to 00h during PWM low time.). During PWM OFF-time then feedback voltage is sampled.
2	stepup2_prot_dis	0	RW	DCDC SU2 overvoltage protection to prevent damage of external NFET, if CURR1, CURR2 or CURR3 feedback selected, and no LED string connected. **0 :** Switch OFF DCDC SU2 if the voltage on FB_SU2 exceeds 1.25V **1 :** Overvoltage protection disabled
1:0	stepup2_fb	'b00	RW	Controls the feedback source **0 :** Voltage feedback (external resistor divider) selected by stepup2_fbprot **1 :** CURR1 feedback enabled (feedback through white LEDs) **2 :** CURR2 feedback enabled (feedback through white LEDs) **3 :** CURR3 feedback enabled (feedback through white LEDs)

Figure 123:
Stepup_control5 Register (Address 54h)

Addr: 54h		Stepup_control5		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	-	'b0000	n/a	Do not use
3	stepup2_pwm_mode	0	RW	Enable PWM mode **0 :** Normal operation **1 :** PWM mode operation. Feedback is sampled during PWM OFF-time, if stpup2_lowf=0.
2	stepup12_clkinv	0	RW	Invert input clock of SU1 and SU2 converter **0 :** Use positive edge of internal clk **1 :** Use negative edge of internal clk
1:0	stepup2_fbprot	'b00	RW	Controls the feedback protection of SU2 with external resistor divider (regulated to 0.8V). **0 :** LX_SD4 enabled as input (If SD4 not used) **1 :** GPIO2 enabled as input **2 :** GPIO3 enabled as input **3 :** GPIO4 enabled as input

Figure 124:
RTCcontrol Register (Address 60h)

Addr: 60h		RTCcontrol		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	-	'b000	n/a	Do not use
4:3	rtc_irq_mode	'b00	RW	**0 :** Generates an interrupt every second **1 :** Generates an interrupt every minute **2 :** Generates an interrupt every 2 minute **3 :** Generates an interrupt every 8 minute
2	rtc_on	0	RW	Switch ON the 32kHz RTC oscillator **0 :** 32kHz oscillator disabled **1 :** 32kHz oscillator enabled
1	rtc_alarm_wakeup_en	0	RW	**0 :** Disables RTC alarm wake-up in power OFF mode **1 :** Enable RTC alarm wake-up in power OFF mode
0	rtc_rep_wakeup_en	0	RW	**0 :** Disables RTC repeated wake-up in power OFF mode **1 :** Enable RTC repeated wake-up in power OFF mode

Figure 125:
RTCSecond Register (Address 61h)

Addr: 61h		RTCSecond		
Bit	Bit Name	Default	Access	Bit Description
7:0	second	00h	RW	-

Figure 126:
RTCMinute1 Register (Address 62h)

Addr: 62h		RTCMinute1		
Bit	Bit Name	Default	Access	Bit Description
7:0	minute0	00h	RW	-

Figure 127:
RTCMinute2 Register (Address 63h)

Addr: 63h		RTCMinute2		
Bit	Bit Name	Default	Access	Bit Description
7:0	minute1	00h	RW	-

Figure 128:
RTCMinute3 Register (Address 64h)

Addr: 64h		RTCMinute3		
Bit	Bit Name	Default	Access	Bit Description
7:0	minute2	00h	RW	-

Figure 129:
RTCAlarmSecond Register (Address 65h)

Addr: 65h		RTCAlarmSecond		
Bit	Bit Name	Default	Access	Bit Description
7:0	alarmsecond	3Fh	RW	AlarmMinute2 has to be written to latch the whole alarm register

Figure 130:
RTCAlarmMinute Register (Address 66h)

Addr: 66h		RTCAlarmMinute		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	alarmminute0	FFh	RW	AlarmMinute2 has to be written to latch the whole alarm register

Figure 131:
RTCAlarmMinute2 Register (Address 67h)

Addr: 67h		RTCAlarmMinute2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	alarmminute1	FFh	RW	AlarmMinute2 has to be written to latch the whole alarm register

Figure 132:
RTCAlarmMinute3 Register (Address 68h)

Addr: 68h		RTCAlarmMinute3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	alarmminute2	FFh	RW	-

Figure 133:
SRAM Register (Address 69h)

Addr: 69h		SRAM		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	SRAM	00h	RW	-

Figure 134:
ADC_control Register (Address 70h)

Addr: 70h		ADC_control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	start_conversion	0	RW	Writing a 1 into this bit starts one ADC conversion
6	adc_on	0	RW	Writing a 1 into this bit continuously activates the ADC S/H and the input multiplexer. The ADC and the MUX are also activated for a conversion period when start_conversion is set to 1. Useful for high impedance input sources on ADC inputs
5	adc_slow	0	RW	Select ADC sampling frequency **0 :** 250kHz (conversion time: approx. 60µs) **1 :** 62.5kHz (conversion time:approx. 240µs)
4	gpio_lv	0	RW	**0 :** High voltage range of GPIO1 to 4/SENSEN_SU1 (4:1 divider active) **1 :** Low voltage range of GPIO1 to 4/SENSEN_SU1 (1:1 divider, 1.8V max)
3:0	adc_select	'b0000	RW	Selects an ADC channel **0 :** BATTEMP NTCADCIN (1:1) **1 :** Temperature sensor: DIE temperature [°C] = adc_result * 0.866 -274 (1:1) **2 :** XOUT32K (1:1, 1.8Vmax) **3 :** CURR1 (1:1, 1V max) **4 :** CURR2 (1:1, 1V max) **5 :** CURR3 (1:1, 1V max) **6 :** VUSB(15:1, 15V max) **7 :** CHGIN (4:1) **8 :** VBAT (4:1) **9 :** VSUP (4:1) **10 :** SENSEN_SU1 (4:1 or 1:1) **11 :** LX_SD4 (4:1 or 1:1) **12 :** GPIO2 (4:1 or 1:1) **13 :** GPIO3 (4:1 or 1:1) **14 :** GPIO4 (4:1 or 1:1) **15 :** NA

Figure 135:
ADC_MSB_result Register (Address 71h)

Addr: 71h		ADC_MSB_result		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	result_not_ready	0	RO	Indicates end of conversion 0 result is ready 1 conversion is running
6:0	D9_3	'b000 0000	RO	ADC result register Bit9 to Bit3

Figure 136:
ADC_LSB_result Register (Address 72h)

Addr: 72h		ADC_LSB_result		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	-	'b0000 0	n/a	Do not use
2:0	D2_0	'b000	RO	ADC result register Bit2 to Bit0

Figure 137:
RegStatus Register (Address 73h)

Addr: 73h		RegStatus		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	curr3_lv	0	RO	Bit is set when voltage of current sink CURR3 drops below low voltage threshold (1ms debounce time default)
6	curr2_lv	0	RO	Bit is set when voltage of current sink CURR2 drops below low voltage threshold (1ms debounce time default)
5	curr1_lv	0	RO	Bit is set when voltage of current sink CURR1 drops below low voltage threshold (1ms debounce time default)
4	-	0	n/a	Do not use
3	sd4_lv	0	RO	Bit is set when voltage of SD4 drops below low voltage threshold (-5%) (1ms debounce time default)
2	sd3_lv	0	RO	Bit is set when voltage of SD3 drops below low voltage threshold (-5%) (1ms debounce time default)
1	sd2_lv	0	RO	Bit is set when voltage of SD2 drops below low voltage threshold (-5%) (1ms debounce time default)
0	sd1_lv	0	RO	Bit is set when voltage of SD1 drops below low voltage threshold (-5%) (1ms debounce time default)

Figure 138:
InterruptMask1 Register (Address 74h)

Addr: 74h		InterruptMask1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	LowBat_int_m	1	RW	**0 :** Interrupt enabled **1 :** Interrupt masked (disabled)
6	ovtmp_int_m	1	RW	**0 :** Interrupt enabled **1 :** Interrupt masked (disabled)
5	onkey_int_m	1	RW	**0 :** Interrupt enabled **1 :** Interrupt masked (disabled)
4	chdet_int_m	1	RW	**0 :** Interrupt enabled **1 :** Interrupt masked (disabled)
3	eoc_int_m	1	RW	**0 :** Interrupt enabled **1 :** Interrupt masked (disabled)
2	resume_int_m	1	RW	**0 :** Interrupt enabled **1 :** Interrupt masked (disabled)
1	nobat_int_m	1	RW	**0 :** Interrupt enabled **1 :** Interrupt masked (disabled)
0	trickle_int_m	1	RW	**0 :** Interrupt enabled **1 :** Interrupt masked (disabled)

Figure 139:
InterruptMask2 Register (Address 75h)

Addr: 75h		InterruptMask2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	rtc_rep_int_m	1	RW	**0 :** Interrupt enabled **1 :** Interrupt masked (disabled)
6	stpup1_det_m	1	RW	**0 :** Interrupt enabled **1 :** Interrupt masked (disabled)
5	stpup1_oc_m	1	RW	**0 :** Interrupt enabled **1 :** Interrupt masked (disabled)
4	bat_temp_m	1	RW	**0 :** Interrupt enabled **1 :** Interrupt masked (disabled)
3	sd4_lv_int_m	1	RW	**0 :** Interrupt enabled **1 :** Interrupt masked (disabled)
2	sd3_lv_int_m	1	RW	**0 :** Interrupt enabled **1 :** Interrupt masked (disabled)
1	sd2_lv_int_m	1	RW	**0 :** Interrupt enabled **1 :** Interrupt masked (disabled)
0	sd1_lv_int_m	1	RW	**0 :** Interrupt enabled **1 :** Interrupt masked (disabled)

Figure 140:
InterruptMask3 Register (Address 76h)

Addr: 76h		InterruptMask3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	-	'b0000 0	n/a	Do not use
2	gpio_restart_int_m	1	RW	**0 :** Interrupt enabled **1 :** Interrupt masked (disabled)
1	gpio_int_m	1	RW	**0 :** Interrupt enabled **1 :** Interrupt masked (disabled)
0	rtc_alarm_int_m	1	RW	**0 :** Interrupt enabled **1 :** Interrupt masked (disabled)

Figure 141:
InterruptStatus1 Register (Address 77h)

Addr: 77h		InterruptStatus1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	LowBat_int_i	0	POP	Bit is set when V_{SUP} drops below ResVoltFall
6	ovtmp_int_i	0	POP	Bit is set when 110deg is exceeded
5	onkey_int_i	0	POP	Rising and falling edge
4	chdet_int_i	0	POP	Rising and falling edge
3	eoc_int_i	0	POP	Rising and falling edge
2	resume_int_i	0	POP	Rising and falling edge
1	nobat_int_i	0	POP	Rising and falling edge
0	trickle_int_i	0	POP	Rising and falling edge

Figure 142:
InterruptStatus2 Register (Address 78h)

Addr: 78h		InterruptStatus2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	rtc_rep_int_i	0	POP	Rising edge only
6	stpup1_det_i	0	POP	Rising edge only
5	stpup1_oc_i	0	POP	Rising edge only
4	bat_temp_i	0	POP	Rising and falling edge
3	sd4_lv_int_i	0	POP	Rising edge only
2	sd3_lv_int_i	0	POP	Rising edge only
1	sd2_lv_int_i	0	POP	Rising edge only
0	sd1_lv_int_i	0	POP	Rising edge only

Figure 143:
InterruptStatus3 Register (Address 79h)

Addr: 79h		InterruptStatus3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	-	'b0000 0	n/a	Do not use
2	gpio_restart_int_i	0	POP	Falling edge
1	gpio_int_i	0	POP	Rising and falling edge
0	rtc_alarm_int_i	0	POP	Rising edge only

Figure 144:
ChargerControl1 Register (Address 80h)

Addr: 80h		ChargerControl1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	nobat_ntc_det	1	RW	Enables nobat_det feature with NTC, ntc_nobat debounce time=100ms
6	auto_resume	1	RW	**0 :** Charger will stay in EOC even when the battery voltage drops **1 :** Charger will start charging when the battery voltage hits the resume level
5	bat_charging_enable	0	RW	**0 :** USB is supplying VSUP, but battery switch is open. USB charger regulates to Vsup_voltage **1 :** Normal battery charger operation form USB charger
4:1	usb_current	'b1000	RW	Sets the USB input current limit, if not GPIO controlled **0 :** 94mA (USB low current, also if gpiox_iosf=12 and gpiox=0) **1 :** 141mA **2 :** 189mA **3 :** 237mA **4 :** 285mA **5 :** 332mA **6 :** 380mA **7 :** 428mA **8 :** 470mA (USB high current, also if gpiox_iosf=12 and gpiox=1) **9 :** 517mA **10 :** 754A **11 :** 1.29A **12 :** 1.7A **13 :** 2.53A **14 :** 2.53A **15 :** 2.53A
0	usb_chgEn	1	RW	ON/OFF control of USB charger input current limiter **0 :** Input current limiter disabled **1 :** Input current limiter enabled

Figure 145:
ChargerVoltageControl Register (Address 81h)

Addr: 81h		ChargerVoltageControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	vsup_min	'b01	RW	Regulate down battery charging current on that level of V_{SUP} during trickle charging and constant current charging, to prevent voltage drop on V_{SUP} **0 :** 3.9V **1 :** 4.2V **2 :** 4.50V **3 :** 4.70V
5:0	ChVoltEOC	'b10 0011	RW	Sets the end-of-charge voltage level V_{CHOFF} (20mV steps) **0 :** 3.5V **1 :** 3.52V **... :** ... **35 :** 4.2V **... :** ... **47-63 :** 4.44V

Figure 146:
ChargerCurrentControl Register (Address 82h)

Addr: 82h		ChargerCurrentControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	eoc_current	0	RW	Sets eoc_current **0 :** eoc current = TrickleCurrent **1 :** eoc current = TrickleCurrent / 2
6	cc_lowlimit	1	RW	Sets the range of the charging current limit in constant current mode. **0 :** Normal mode **1 :** Low current mode Current= ConstantCurrent -500mA
5:2	ConstantCurrent	'b0000	RW	Sets the charging current limit in constant current mode. **0 :** 750mA **1 :** 800mA **2 :** 850mA **3 :** 900mA **4 :** 950mA **5 :** 1000mA **6 :** 1050mA **7 :** 1100mA **8 :** 1150mA **9 :** 1200mA **10 :** 1250mA **11 :** 1300mA **12 :** 1350mA **13 :** 1400mA **14 :** 1450mA **15 :** 1500mA
1:0	TrickleCurrent	'b01	RW	Sets the charging current limit in trickle current mode. **0 :** 60mA **1 :** 120mA **2 :** 180mA **3 :** 240mA

Figure 147:
ChargerConfig Register (Address 83h)

Addr: 83h		ChargerConfig		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	-	0	n/a	Do not use
6	Charging_1Hz_clk	0	RW	Sets the mode for the charging output status (gpioX_iosf=10) **0 :** Normal operation: charging=1, not charging=0 **1 :** 1Hz blinking operation: charging=1Hz, not charging=0
5	ChVoltResume	0	RW	Sets the resume voltage level V_{CHRES}. **0 :** 120mV **1 :** 240mV
4:3	temp_sel	'b00	RW	Selects temperature regulation of charging current (die temperature) **0 :** 110°C **1 :** 90°C **2 :** 120°C **3 :** 130°C
2:0	vsup_voltage	'b101	RW	Voltage regulation of VSUP of the input current limiter **0 :** 4.4V **1 :** 4.5V **2 :** 4.6V **3 :** 4.7V **4 :** 4.8V **5 :** 4.9V **6 :** 5.0V **7 :** 5.5V

Figure 148:
NTCsupervision Register (Address 84h)

Addr: 84h		NTCsupervision		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	-	'b0000 0	n/a	Do not use
2	ntc_temp	0	RW	Select NTC mode **0 :** 50deg temperature limit **1 :** 45deg temperature limit
1	ntc_10k	0	RW	Select NTC resistor type **0 :** 100kΩ **1 :** 10kΩ
0	ntc_on	0	RW	ON/OFF control of battery NTC supervision **0 :** Disabled **1 :** Enabled

Figure 149:
Chargersupervision Register (Address 85h)

Addr: 85h		Chargersupervision		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	-	0	n/a	Do not use
6	ovprot_dis	0	RW	Disables external overvoltage protection, function of XOFF pin **0 :** Overvoltage protection enabled **1 :** Overvoltage protection disabled
5	dcdc_chmode	1	RW	Enables DCDC charger mode **0 :** Linear charger mode enabled **1 :** Step down charger enabled
4	charging_tmax	1	RW	**0 :** Read: no time-out reached, Write: reset charger time-out counter **1 :** ch_timeout reached and charging stopped
3:0	ch_timeout	'b0000	RW	Sets the charger time-out timer **0 :** OFF **1 :** 0.5 hour **2 :** 1 hour **3 :** 1.5 hour **4 :** 2 hour **5 :** 2.5 hour **6 :** 3 hour **7 :** 3.5 hour **8 :** 4 hour **9 :** 4.5 hour **10 :** 5 hour **11 :** 5.5 hour **12 :** 6 hour **13 :** 6.5 hour **14 :** 7 hour **15 :** 7.5 hour

Figure 150:
ChargerStatus1 Register (Address 86h)

Addr: 86h		ChargerStatus1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Nobat	0	RO	Bit is set, if no battery has been detected (after EOC measured on NTC)
6	Battemp_hi	0	RO	Bit is set, if high battery temperature has been detected
5	EOC	0	RO	Bit is set, if End of charge state has been reached
4	CVM	0	RO	Bit is set, if charger is operating in constant voltage mode
3	Trickle	0	RO	Bit is set, if charger is operating in trickle current. $V_{BAT} < 2.9V$
2	Resume	0	RO	Bit is set, if Battery voltage is below resume level
1	CCM	0	RO	Bit is set, if charger is operating in constant current mode
0	ChDet	0	RO	Bit is set when external charge adapter has been detected on pin $V_{CHARGER}$

Figure 151:
ChargerStatus2 Register (Address 87h)

Addr: 87h		ChargerStatus2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	-	‘b0000 0	n/a	Do not use
2	usb_prot_ready	0	RO	Bit indicates, that the USB input voltage protection pin X_{OFF} is precharged to a voltage > 7.5V X_{OFF} is pull to GND if an overvoltage on V_{USB} is detected.
1	batsw_on	0	RO	Bits indicates the status of the battery switch **00 :** Battery switch closed **01 :** Battery switch open with ideal diode **10 :** Charging mode **11 :** Battery switch closed
0	batsw_mode	0	RO	

Figure 152:
Lock Register (Address 8eh)

Addr: 8eh		Lock		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	-	‘b0000 0	n/a	Do not use
2	charger_lock	0	RW	Enables lock of the following charger registers: 81h, 82h, 83h, Chargervoltagecontrol, Chargercurrentcontrol, Chargerconfig. Bits can only be set. Reset only with full reset cycle
1:0	reg_lock	'b00	RW	Enables lock of Regulator voltages Bits can only be set. Reset only with full reset cycle **0 :** No lock **1 :** Lock of voltage of LDOs (LDO1..8_vsel) (all bits) and voltage of StepDownBits(sd1..4_vsel) [5:6] only **2 :** Lock voltage of StepDownbits 5:6 only (no LDOs) **3 :** Lock voltage of StepDowns (all bits) and LDOs (all bits). **Note:** Setting sdx_vsel to 0 is possible all the time to allow switching OFF the regulator. Writing a non-zero value after that will restore the old value.

Figure 153:
ASIC_ID1 Register (Address 90h)

Addr: 90h		ASIC_ID1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ID1	8Bh	RO	-

Figure 154:
ASIC_ID2 Register (Address 91h)

Addr: 91h		ASIC_ID2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3:0	revision	'b0001	RO	For chip version 2v1 (metal fuse)

Application Information

Figure 155:
AS3711 Application Schematic

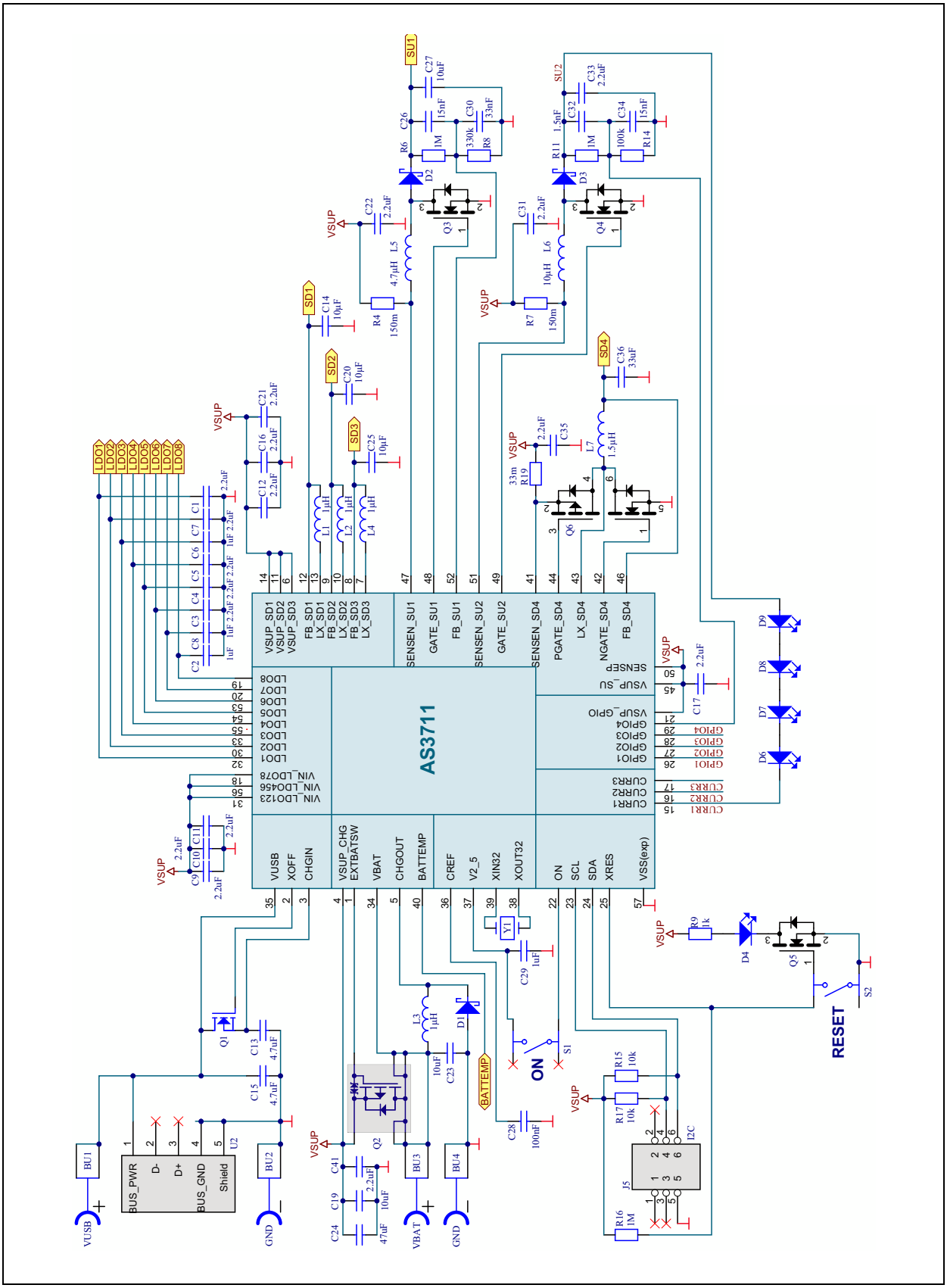


Figure 156:
PCB Layout Recommendation for SD1, SD2, SD3 and Switched Mode Charger

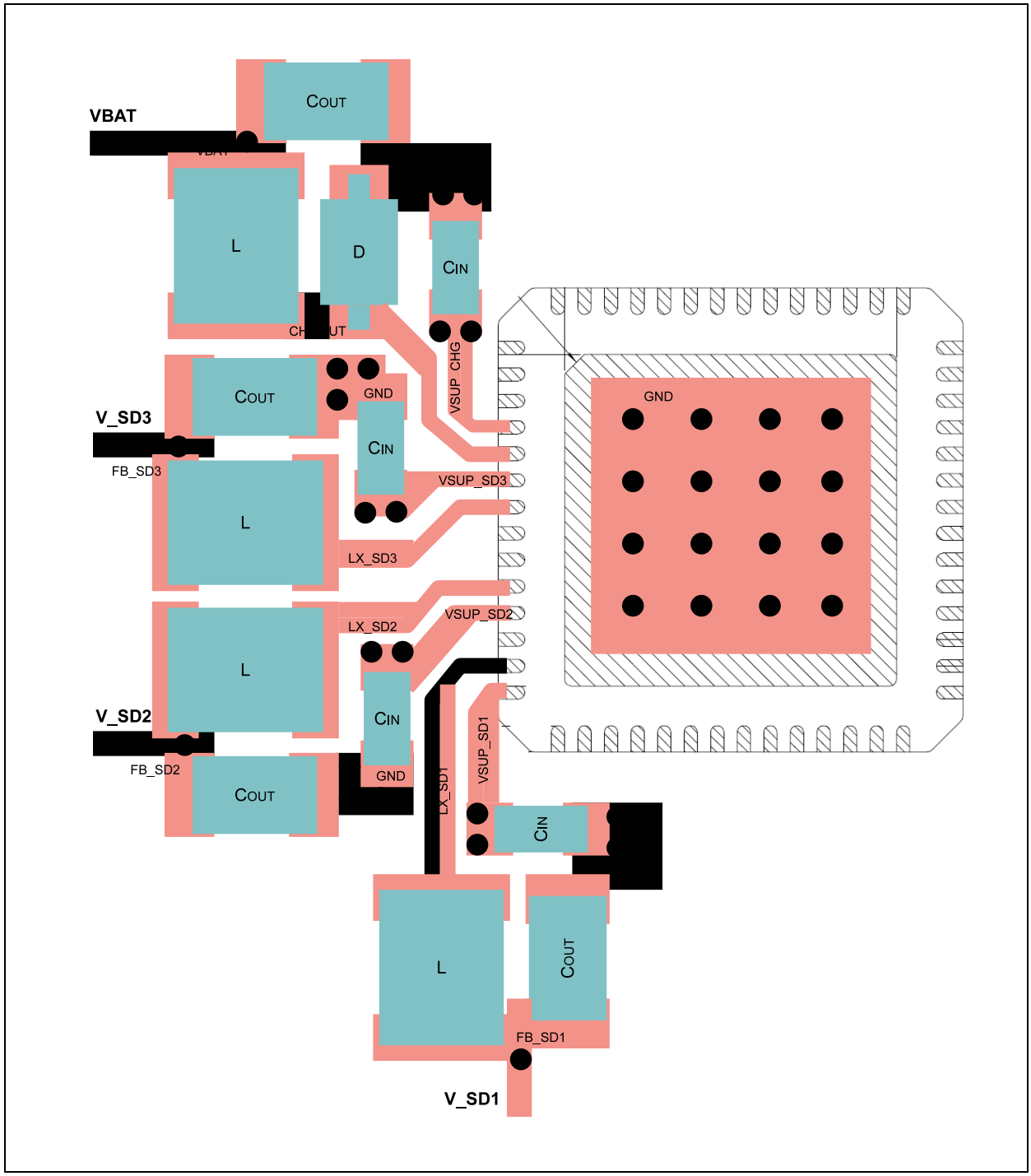
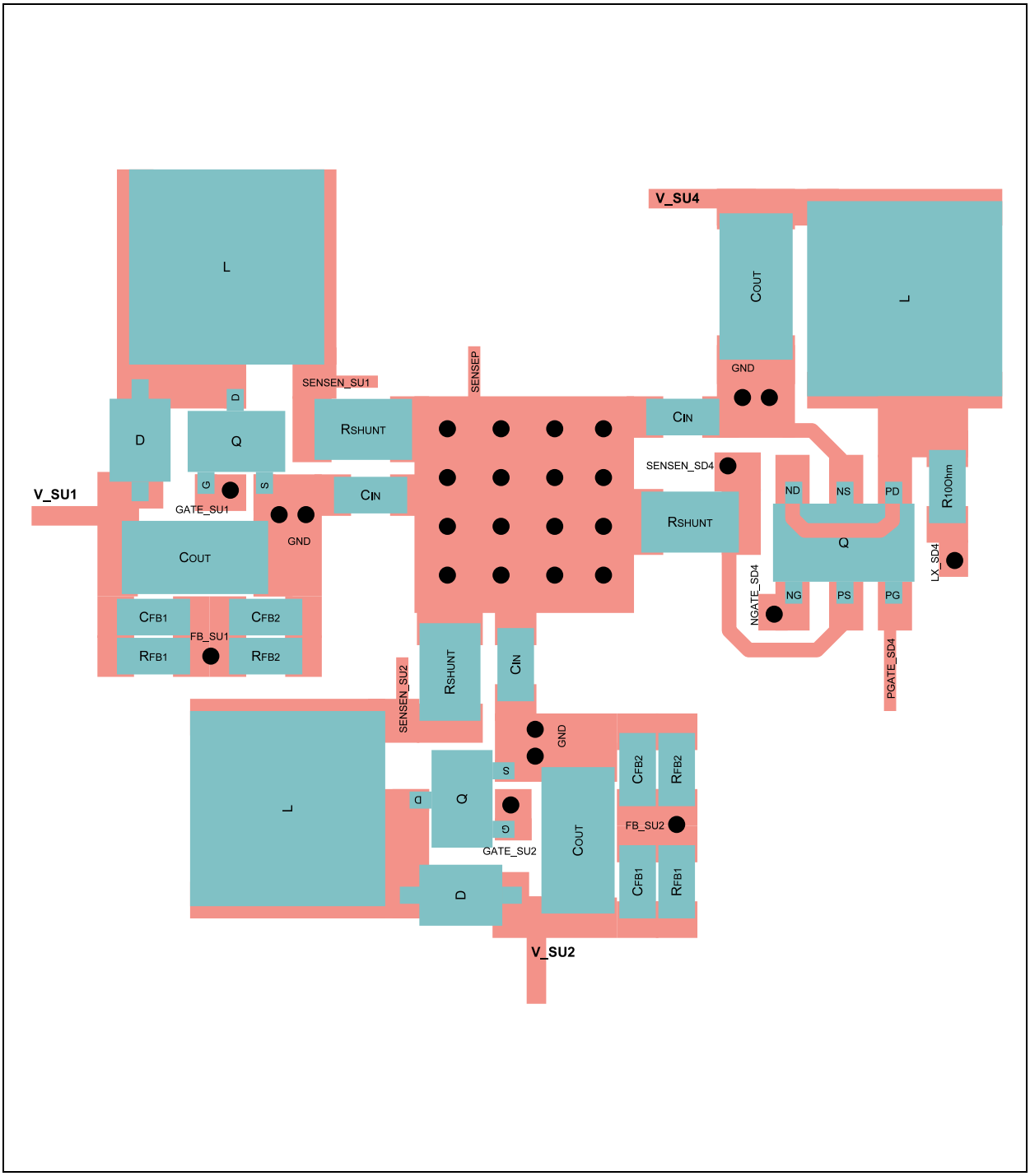
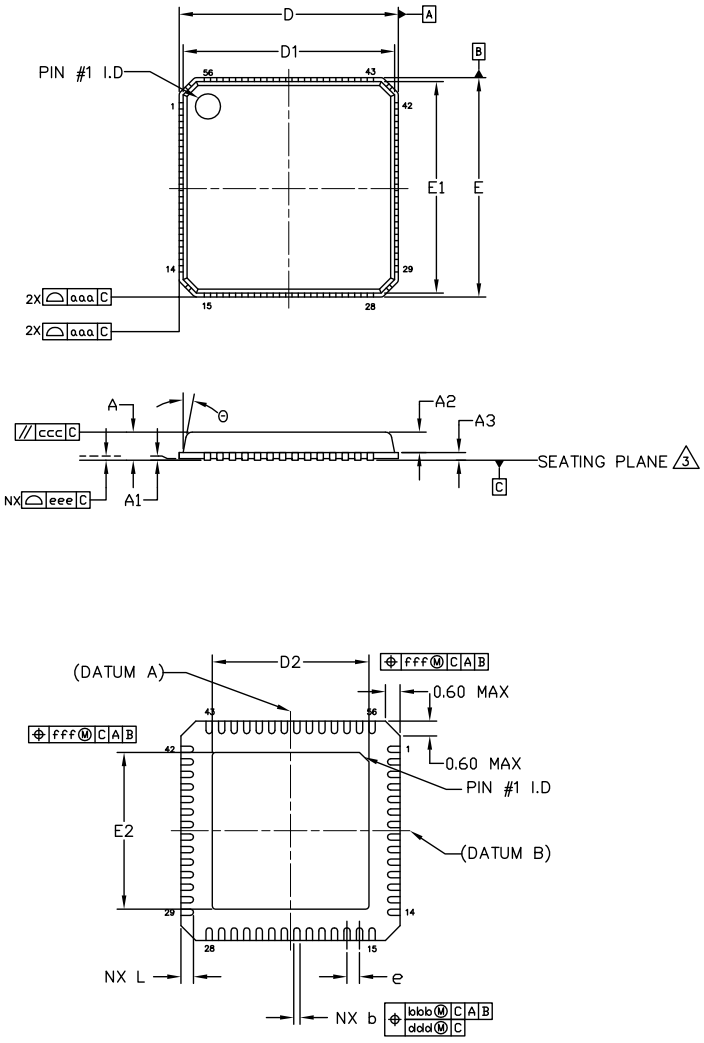


Figure 157:
PCB Layout Recommendation for SU1, SU2, SD4



Package Drawings & Markings

Figure 158:
Package Drawings and Dimensions QFN56

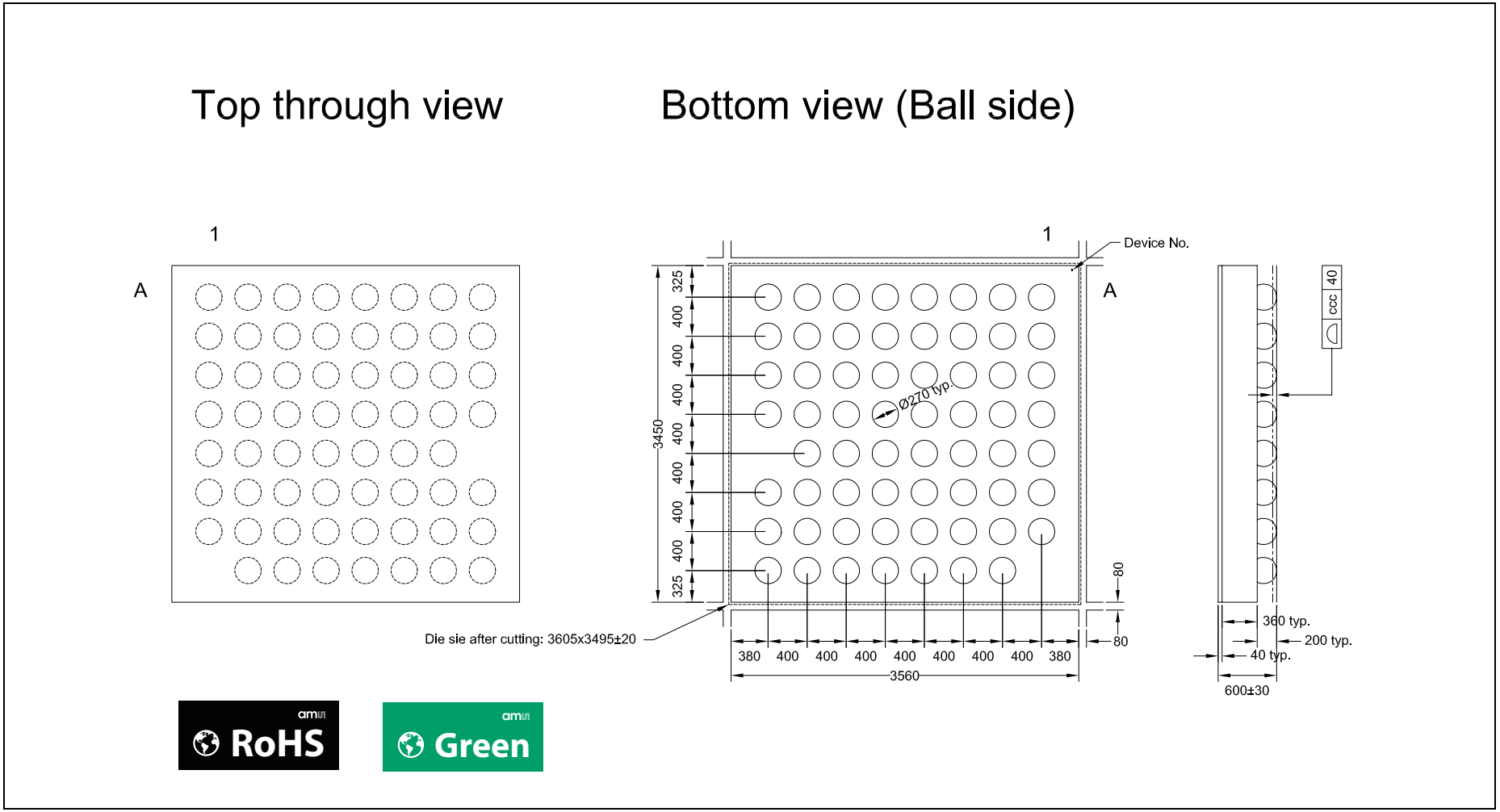


Symbol	Min	Nom	Max
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	-	0.65	1.00
A3	-	0.20REF	-
L	0.35	0.40	0.45
Θ	0°	-	14°
b	0.15	0.20	0.25
D		7.00BSC	
E		7.00BSC	
e		0.40BSC	
D2	4.90	5.00	5.10
E2	4.90	5.00	5.10
D1	-	6.75BSC	-
E1	-	6.75BSC	-
aaa	-	0.10	-
bbb	-	0.07	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N		56	

Note(s) and/or Footnote(s):

1. Dimensions and tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Coplanarity applies to the exposed heat slug as well the terminal.
4. Radius on the terminal is optional.
5. N is the total number of the terminal.

Figure 159:
Package Drawings and Dimensions CSP64



Note(s) and/or Footnote(s):

1. Pin 1 = A1
2. ccc Coplanarity
3. All dimensions are in µm

Figure 160:
Marking

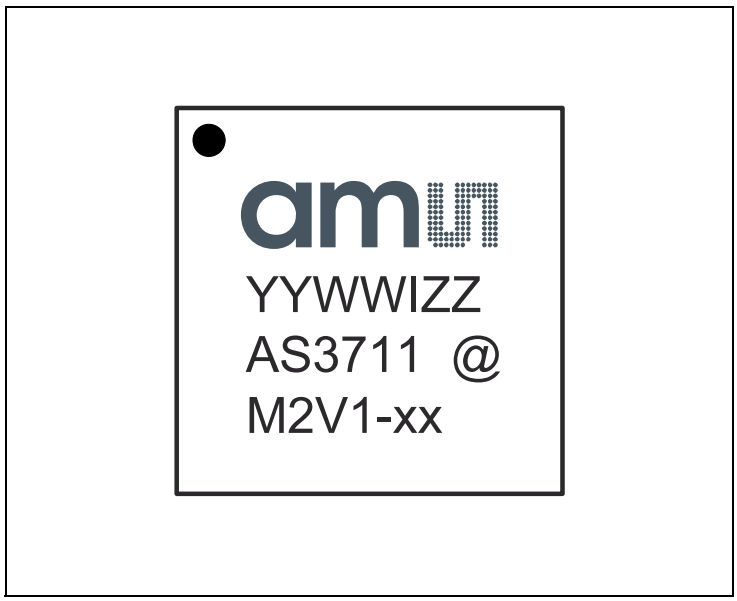


Figure 161:
Package Code YYWWIZZ

YY	WW	I	ZZ	@
Year	Working week assembly / packaging	Plant identifier	Free choice	Sublot Identifier (for QFN only)

Figure 162:
Start-up Revision Code

xx	Sequence
FF	Engineering samples, no sequence programmed or sequence programmed on request
00	Default sequence (no sequence programmed)
xx	Customer specified sequence programmed during production test

Ordering & Contact Information

The devices shown in Figure 163 are available as standard products.

Figure 163:
Ordering Information

Part Number	Marking	Sequence	Description	Delivery Form	Package
AS3711-BQFR-FF	M2V1-FF	Sequence programmable on request	Quad Buck High Current PMIC with Charger	Tape & Reel dry pack	QFN56 7×7 0.4mm pitch
AS3711-BQFP-00	M2V1-00	Default sequence	Quad Buck High Current PMIC with Charger	Tape & Reel dry pack	QFN56 7×7 0.4mm pitch
AS3711-BQFP-xx	M2V1-xx	Customer specified	Quad Buck High Current PMIC with Charger	Tape & Reel dry pack	QFN56 7×7 0.4mm pitch
AS3711-BWLT-FF	M2V1-FF	Sequence programmable on request	Quad Buck High Current PMIC with Charger	Tape & Reel	WL-CSP64, 0.4mm pitch
AS3711-BWLT-00	M2V1-00	Default sequence	Quad Buck High Current PMIC with Charger	Tape & Reel	WL-CSP64, 0.4mm pitch
AS3711-BWLT-xx	M2V1-xx	Customer specified	Quad Buck High Current PMIC with Charger	Tape & Reel	WL-CSP64, 0.4mm pitch

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Document Status	Product Status	Definition
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Revision Information

Changes from 1.2 (2012-May) to current revision 1-34 (2014-Nov-10)	Page
Content of austriamicrosystems datasheet was updated to latest **ams** design	
Added CSP package information to the datasheet	
Added benefits and CSP package to Figure 1	2
Updated QFN blockdiagram (Figure 2)	4
Added CSP block diagram (Figure 3)	5
Added Ball Assignment CSP (Figure 5)	7
Added CSP ball info. and updated pins VINLDO78, XRES, VINLDO456 & VSSA (Figure 6)	7
Updated Figure 7	11
Added $C_{load\_LDO3\text{-}8\_L}$ & $C_{load\_LDO3\text{-}8\_H}$ parameters to Figure 28	29
Added I_{out} to Figure 29	31
Updated text under DCDC Step-Up Converter	32
Renamed VFB2 to VCURR in Figure 35	38
Updated $I_{CURR1,2,3}$ in Figure 39 and text under Current Sinks	40
Updated text under Charger	41
Updated text under NTC supervision	45
Updated Figure 51	53
Renamed VXRES to VRES in Figure 52	54
Updated Figure 54	57
Updated descriptions of IO Functions	59
Updated sections Vselect Input & Stand-by and Vselect input	60
Updated Figure 62	67
Updated description of Real Time Clock	69
Replaced osc_pd=1with rtc_on=0 in GPIO1-,GPIO2-,GPIO3-, GPIO4- control registers	86 - 89
Replaced osc_pd=1with rtc_on=0 in curr_control register	105
Changed 0.15mA to 0.1562mA and 38.25 to 39.84 in curr1-,curr2-, curr3_value registers	106 - 107
Updated bit 6 in Chargersupervision register	126

Changes from 1.2 (2012-May) to current revision 1-34 (2014-Nov-10)	Page
Updated ASIC_ID2 Register	128
Updated Figure 159	133
Updated Figure 160 & Figure 161	134
Updated Figure 163	135

Note(s) and/or Footnote(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide